

LCFC Confidential

TGL-U LCFC T/S Schematics Document

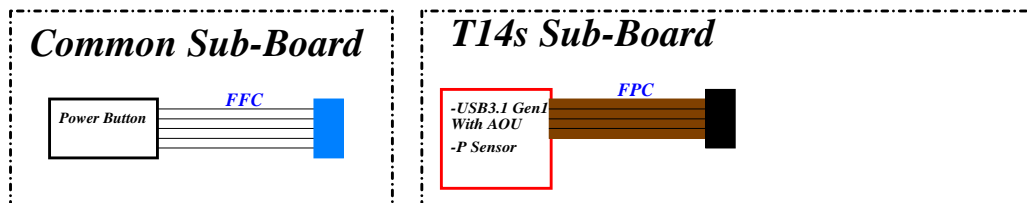
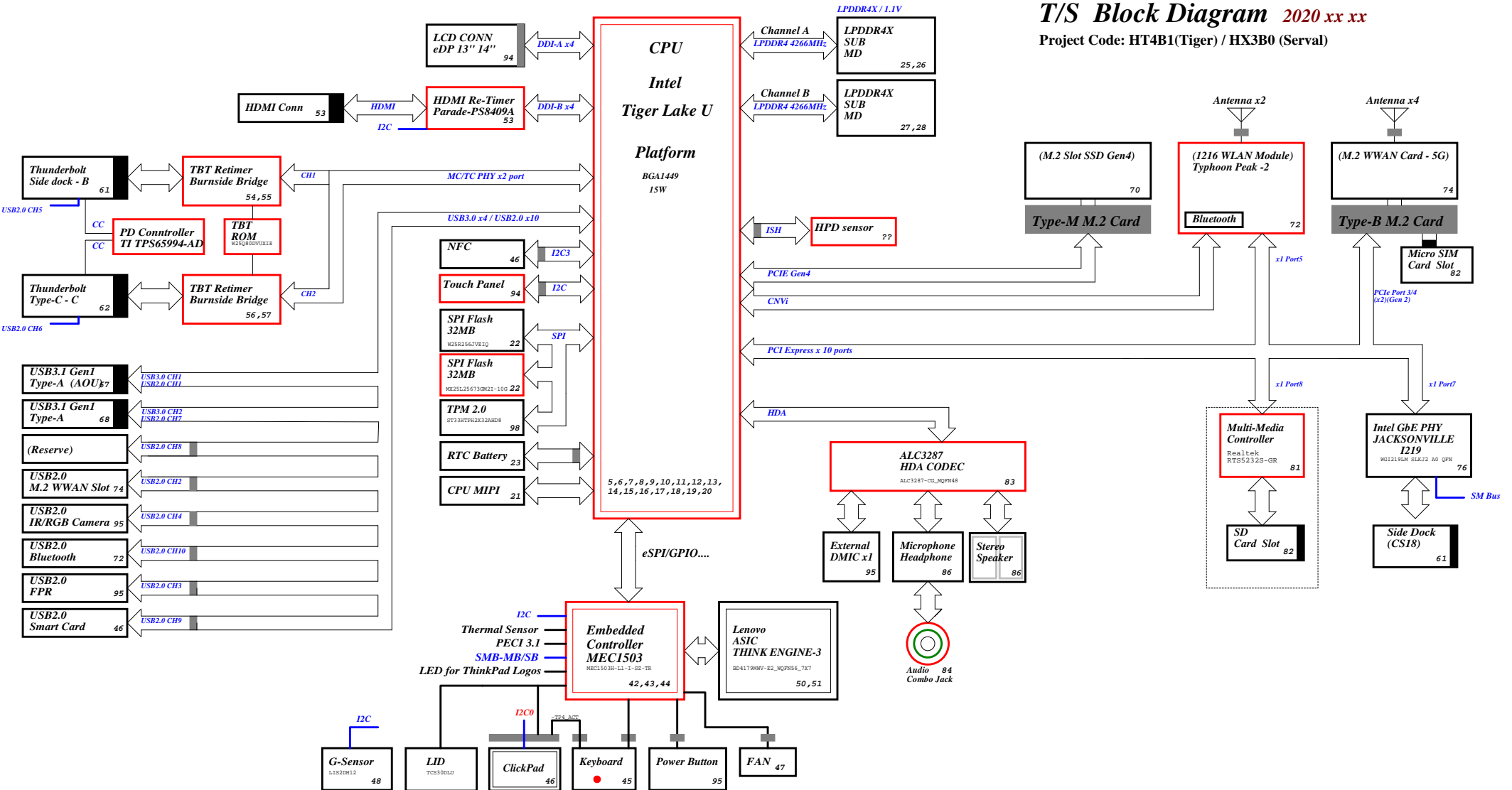
Tiger / Serval M/B SCHEMATICS

Intel TigerLake Processy with LPDDR4X

REV:0.03

T/S Block Diagram 2020 xx xx

Project Code: HT4B1(Tiger) / HX3B0 (Serval)



- Sub Board
- Different with CS20
- External Connector/Socket
- Internal Connector/Socket
- Internal Switch

607872_TGL_UP3_UP4_PltDoc_Rev1p5

10.12.4 Power States

Table 237. System with M3 State Supported

| Rails | SKU s | S0/M0 ³ | C10 ² | S0ix/M- off ⁴ | S4 and S5/M3 | S4 and S5/M- off | Deep S4/S5 | G3 ¹ |
|---------------------|----------|--------------------|------------------|-----------------------------|-----------------|---------------------|---------------|-----------------|
| VCCRTC | All | ON | ON | ON | ON | ON | ON | ON |
| VCCDSW_3P3 | All | ON | ON | ON | ON | ON | ON | No Power |
| VBATA (VDC) | All | ON | ON | ON | ON | ON | ON | No Power |
| V5.0A | All | ON | ON | ON | ON | ON | OFF | No Power |
| VCCPRIM_3P3 | All | ON | ON | ON | ON | ON | OFF | No Power |
| VCCPRIM_1P8 | All | ON | ON | ON | ON | ON | OFF | No Power |
| VCC_VNNEXT_1P0 5 | All | ON | ON | ON | ON | ON | OFF | No Power |
| continued... | | | | | | | | |

| Rails | SKU s | S0/M0 ³ | C10 ² | S0ix/M- off ⁴ | S4 and S5/M3 | S4 and S5/M- off | Deep S4/S5 | G3 ¹ |
|-----------------------|----------|--------------------|------------------|-----------------------------|-------------------|---------------------|---------------|-----------------|
| VCC_V1P05EXT_1 P05 | All | ON | ON | ON | ON | ON | OFF | No Power |
| V3.3M ⁵ | All | ON | ON | OFF | ON ¹⁰ | OFF | OFF | No Power |
| V1.8M ⁵ | All | ON | ON | OFF | ON ¹⁰ | OFF | OFF | No Power |
| VDDQ | All | ON | ON | ON | OFF | OFF | OFF | No Power |
| V2.5U (VPP) | All | ON | ON | ON | OFF | OFF | OFF | No Power |
| VCCST | All | ON | ON | ON | OFF ⁶ | OFF ⁶ | OFF | No Power |
| VCCSTG | All | ON | OFF ² | OFF | OFF | OFF | OFF | No Power |
| VCC1P8A ¹⁵ | H | ON | OFF | OFF | OFF | OFF | OFF | No Power |
| V3.3S | All | ON | ON | ON | OFF | OFF | OFF | No Power |
| VCCIN | All | ON | ON | ON ¹¹ | OFF | OFF | OFF | No Power |
| VCCIN_AUX | All | ON | ON | ON ¹¹ | OFF ¹⁴ | OFF ¹⁴ | OFF | No Power |

- Notes: 1. The state of the system without RTC well powered can also be considered G3.
2. VCCSTG can be turned off when the processor is in C10
3. S0/M0 state includes all Package C-states from C0-C10
4. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCH
5. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not used directly by the CPU/PCH, and are not present on non-M3 supported systems
6. VCCST and VCCSTG can remain powered during S4 and S5 power states for board cost optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Platform Debug and Test Hooks chapter for more details.
7. NA
8. NA
9. VCCSTG is allowed to be ramped to 0V during S0 only when CPU_C10_GATE# is asserted. Specific exit latency targets are required when this feature is implemented. If VCCSTG power gating is not supported on the platform (shared with VCCST), VCCSTG is allowed to stay ON during S0ix states. Note that merging power rails may reduce power optimization opportunities on the platform.
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. This supply is expected to be 0V during states where SLP_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it is lowest power consumption. Specific power up latencies apply when exiting this state. Applicable to form factors with battery only (ie. AIC)Optional depending platform design; ON if AC is present

Title

<Title>

Size A

Document Number
T14s Gen2

Rev
0.1

Date:

Friday, December 18, 2020

Sheet 3 of 130

T/S SIT Planar Logic Schematics

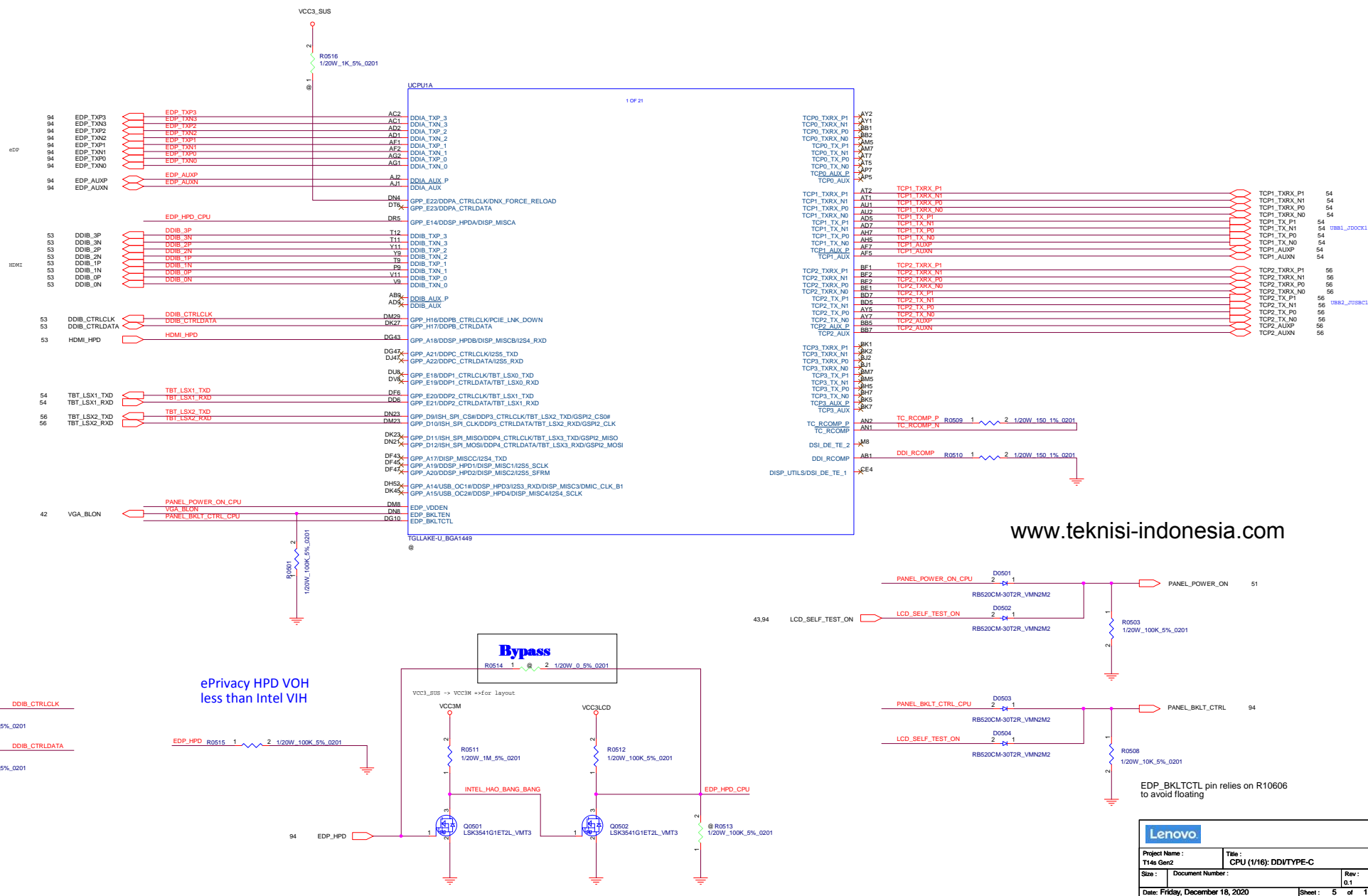
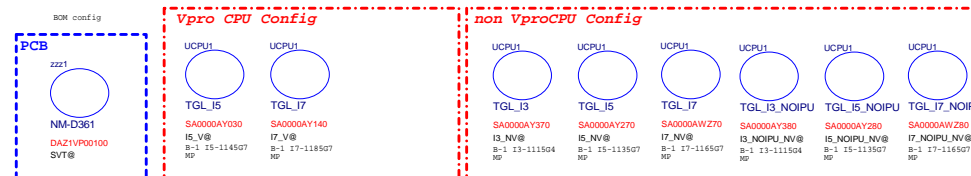
T/S
VER 1.00
Sep/06/2020

BASE LOGIC : T14s GEN2_FVT_0803_V20_final_BOM

| | |
|------------------------------------|---------------------------------|
| 1.Project Name | 36.BLANK |
| 2.BLOCK DIAGRAM | 37.BLANK |
| 3.EC list | 38.BLANK |
| 4.TITLE PAGE | 39.BLANK |
| 5.CPU(1/16) : DDI/EDP | 40.BLANK |
| 6.CPU(2/16) : DDR (1/2) | 41.BLANK |
| 7.CPU(3/16) : DDR (2/2) | 42.MEC1503 (1/3) |
| 8.CPU(4/16) : MISC/JTAG | 43.MEC1503 (2/3) |
| 9.CPU(5/16) : LPC/SPI/SMBUS/C-LINK | 44.MEC1503 (3/3) |
| 10.CPU(6/16) : LPSS/ISH | 45.KEYBOARD/TRACK POINT |
| 11.CPU(7/16) : AUDIO | 46.TOUCH PAD/Smart card/NFC |
| 12.CPU(8/16) : PCIE/USB/SATA | 47.FAN CONNECTOR |
| 13.CPU(9/16) : CSI-2/EMMC/CNVI | 48.APS G-SENSOR |
| 14.CPU(10/16) : CLOCK SIGNALS | 49.BLANK |
| 15.CPU(11/16) : SYSTEM PM | 50.THINK ENGINE-3 (1/2) |
| 16.CPU(12/16) : CPU POWER (1/2) | 51.THINK ENGINE-3 (2/2) |
| 17.CPU(13/16) : CPU POWER (2/2) | 52.BLANK |
| 18.CPU(14/16) : PCH POWER | 53.HDMI CONNECTOR |
| 19.CPU(15/16) : GND | 54.THUNDERBOLT RETIMER B (1/2) |
| 20.CPU(16/16) : CFG/RESERVED | 55.THUNDERBOLT RETIMER B (2/2) |
| 21.MIPI60 DEBUG PORT | 56.THUNDERBOLT RETIMER C (1/2) |
| 22.SPI FLASH | 57.THUNDERBOLT RETIMER C (2/2) |
| 23.RTC | 58.BLANK |
| 24.BLANK | 59.USB PD CONTROLLER |
| 25.LPDDR4X CHANNEL 0&1 | 60.BLANK |
| 26.LPDDR4X CHANNEL 2&3 | 61.TYPE-C with THUNDERBOLT |
| 27.LPDDR4X CHANNEL 4&5 | 62.TYPE-C with DOCK/THUNDERBOLT |
| 28.LPDDR4X CHANNEL 6&7 | 63.BLANK |
| 29.BLANK | 64.BLANK |
| 30.BLANK | 65.TYPESC_DCIN |
| 31.BLANK | 66.BLANK |
| 32.BLANK | 67.USB TYPE-A CONNECTOR |
| 33.BLANK | 68.USB TYPE-A CONN |
| 34.BLANK | 69.BLANK |
| 35.BLANK | 70.M.2 SOCKET 3 MODULE I/F |

| | |
|------------------------------------|----------------------------------|
| 71.BLANK | 101.BATTERY INPUT |
| 72.M.2 TYPE 1216 MODULE | 102.BATTERY CHARGER |
| 73.BLANK | 103.DC/DC VCC5M |
| 74.M.2 SOCKET 2 MODULE I/F | 104.BLANK |
| 75.BLANK | 105.DC/DC VCC3M |
| 76.GBE JACKSONVILLE | 106DC/DC VCC1R2A/2R5A |
| 77.BLANK | 107.DC/DC VCC5M_PD |
| 78.BLANK | 108.DC/DC VCCCPUCORE (MP2940A) |
| 79.BLANK | 109.DC/DC VCCCPUCORE (MP86941*2) |
| 80.BLANK | 110.DC/DC VCCCPUCORE (MP86941*1) |
| 81.MEDIA CARD CONTROLLER | 111.DC/DC VCCPCHCORE(MP2941B) |
| 82.MEDIA CARD INTERFACE | 112.BLANK |
| 83.AUDIO CONNECTOR | 113.BLANK |
| 84.AUDIO SMART AMP | 114.DC/DC VCC1R8_SUS |
| 85.AUDIO SPEAKER | 115.BLANK |
| 86.AUDIO BEEP | 116.BLANK |
| 87.BLANK | 117.BLANK |
| 88.BLANK | 118.BLANK |
| 89.BLANK | 119.BLANK |
| 90.BLANK | 120.LOAD SW VCC3_SUS |
| 91.BLANK | 121.LOAD SW LAN |
| 92.BLANK | 122.LOAD SW B |
| 93.SMART CARD READER | 123.LOAD SW TOUCH PANEL & SSD |
| 94.LCD & TOUCH PANEL INTERFACE | 124.BLANK |
| 95.LID/CAMERA/MIC/SENSOR INTERFACE | 125.BLANK |
| 96.BLANK | |
| 97.BLANK | |
| 98.DISCRETE TPM 2.0 | |
| 99.BLANK | |
| 100.DC-INPUT | |

| | |
|--|--|
| GPP_E19/DDP1_CTRLDATA/TBT_LXS0_RXD (DDP1 I2C / TBT_LXS0 Pin VCC Configuration) | |
| GPP_E21/DDP2_CTRLDATA/TBT_LXS1_RXD (DDP2 I2C / TBT_LXS1 Pin VCC Configuration) | |
| GPP_D10/DDP3_CTRLDATA/TBT_LXS2_RXD (DDP3 I2C / TBT_LXS2 Pin VCC Configuration) | |
| GPP_D12/DDP4_CTRLDATA/TBT_LXS3_RXD (DDP4 I2C / TBT_LXS3 Pin VCC Configuration) | |
| HIGH | 3.3V for HDMI Display I2C (External Pull-Up Resistor Required) |
| LOW | 1.8V for Thunderbolt LXS (Default) |



| SPI0_MOSI (Boot Halt) | |
|-----------------------|----------|
| HIGH | Disabled |
| LOW | Enabled |

← LOGIC

| SPI0_I02 (Consent Strap) | |
|--------------------------|----------|
| HIGH | Disabled |
| LOW | Enabled |

← LOGIC

| SPI0_IO3 (A0 Personality Strap) | |
|---------------------------------|----------|
| HIGH | Disabled |
| LOW | Enabled |

← LOGIC

| GPP_E6 (JTAG ODT Disable) | |
|---------------------------|-------------------|
| HIGH | JTAG ODT Enabled |
| LOW | JTAG ODT Disabled |

← LOGIC

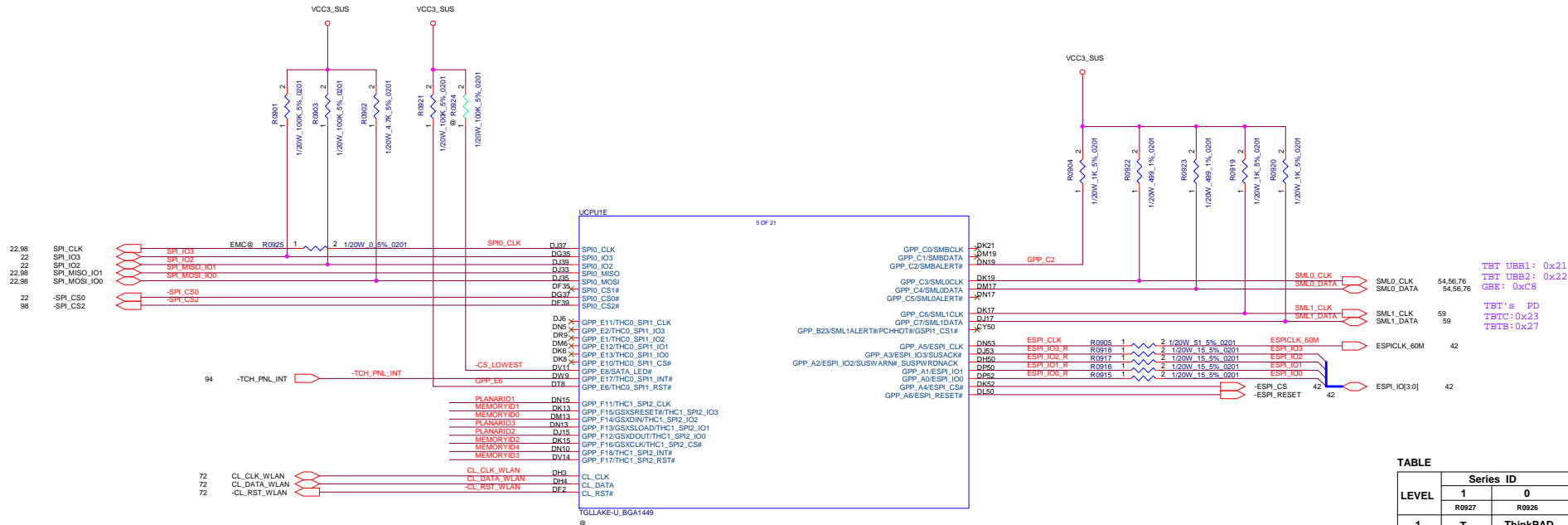
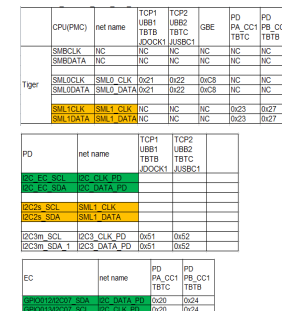
| GPP_C2/SMBALERT# (TLS Confidentiality) | |
|--|---|
| HIGH | Enable ME Crypto TLS with Confidentiality |
| LOW | Disable ME Crypto TLS (Default) |

← LOGIC

| | |
|--------------------------------------|---|
| GPP_C5/SML0ALERT# (Boot Strap Bit 0) | |
| GPP_H0 (Boot Strap Bit 1) | |
| GPP_H1 (Boot Strap Bit 2) | |
| GPP_H2 (Boot Strap Bit 3) | |
| 0000b | Master Attached Flash Configuration (Default) |

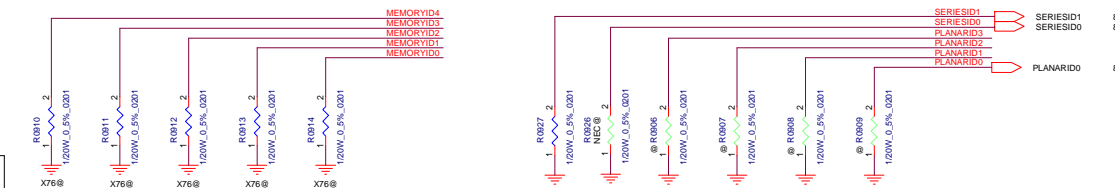
| GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency) | |
|--|---|
| HIGH | 19.2MHz Clock (Derived from 38.4MHz Crystal) |
| LOW | 38.4MHz Clock (Direct from Crystal) (Default) |

← LOGIC



| LEVEL | MEMORY ID | | | | |
|-------|-----------|-------|-------|-------|-------|
| | 4 | 3 | 2 | 1 | 0 |
| | R0910 | R0911 | R0912 | R0913 | R0914 |
| 1 | NA | NA | NA | NA | NA |
| 0 | ASM | ASM | ASM | ASM | ASM |


| MEMORYID[4:0] | U2501,U2601,U2701,U2801 | | | | Total Memory | LCFC PN |
|---------------|-------------------------|--------------------------|----------|-----|--------------|-------------|
| | Supplier | Supplier's P/N | Capacity | | | |
| 00h (00000b) | SK hynix | H9HCNNNBKMLLR-XR-NEE | 16Gb | DDP | 8GB | SA0000AAM10 |
| 01h (00001b) | | H9HCNNNCPMLLR-XR-NEE | 32Gb | QDP | 16GB | SA0000AMB10 |
| 02h (00010b) | | H9HCNNNFAMMLLR-XR-NEE | 64Gb | QDP | 32GB | SA0000AXB00 |
| 03h (00011b) | | K4U6E3S4AA-MGCR | 16Gb | SDP | 8GB | SA0000AMP10 |
| 04h (00100b) | Samsung | K4UBE3D4AA-MGCR | 32Gb | DDP | 16GB | SA0000AMG10 |
| 05h (00101b) | | K4UCJE3Q4AA-MGCR | 64Gb | QDP | 32GB | SA0000AMR10 |
| 06h (00110b) | Micron | MT53E512M32D2NP-046 WT:E | 16Gb | DDP | 8GB | SA00009ET00 |
| 07h (00111b) | | MT53E1G32D2NP-046 WT:A | 32Gb | DDP | 16GB | SA0000ANA10 |
| 08h (00100b) | | MT53E2G32D2ANQ-046 WT:A | 64Gb | QDP | 32GB | SA0000AN910 |



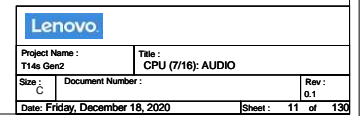
| LEVEL | Series ID | |
|-------|-----------|----------|
| | 1 | 0 |
| | R0927 | R0926 |
| 1 | T | ThinkPAD |
| 0 | Ts/X | NEC |

| LEVEL | PLANAR ID | | | |
|-------|-----------|-------|-------|-------|
| | 3 | 2 | 1 | 0 |
| | R0906 | R0907 | R0908 | R0909 |
| 1 | NA | NA | NA | NA |
| 0 | ASM | ASM | ASM | ASM |

| LEVEL | PLANARID[3:0] |
|-------|---------------|
| EVT | 0000b |
| FVT | 0001b |
| SIT | 0100b |
| SVT | 1111b |

| | | |
|---|--------------------------|--|
|  | | |
| Project Name : T14s Gen2 | | Title : CPU (5/16): ESP/SP/SMBS/C-LINK |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 9 of 130 |

| | |
|------------------------------------|--|
| GPP_R2/HDA_SDO/I2S0_TXD | |
| Flash Descriptor Security Override | |
| HIGH | Disable Flash Descriptor Security (Override) |
| LOW | Enable Flash Descriptor Security (Default) |



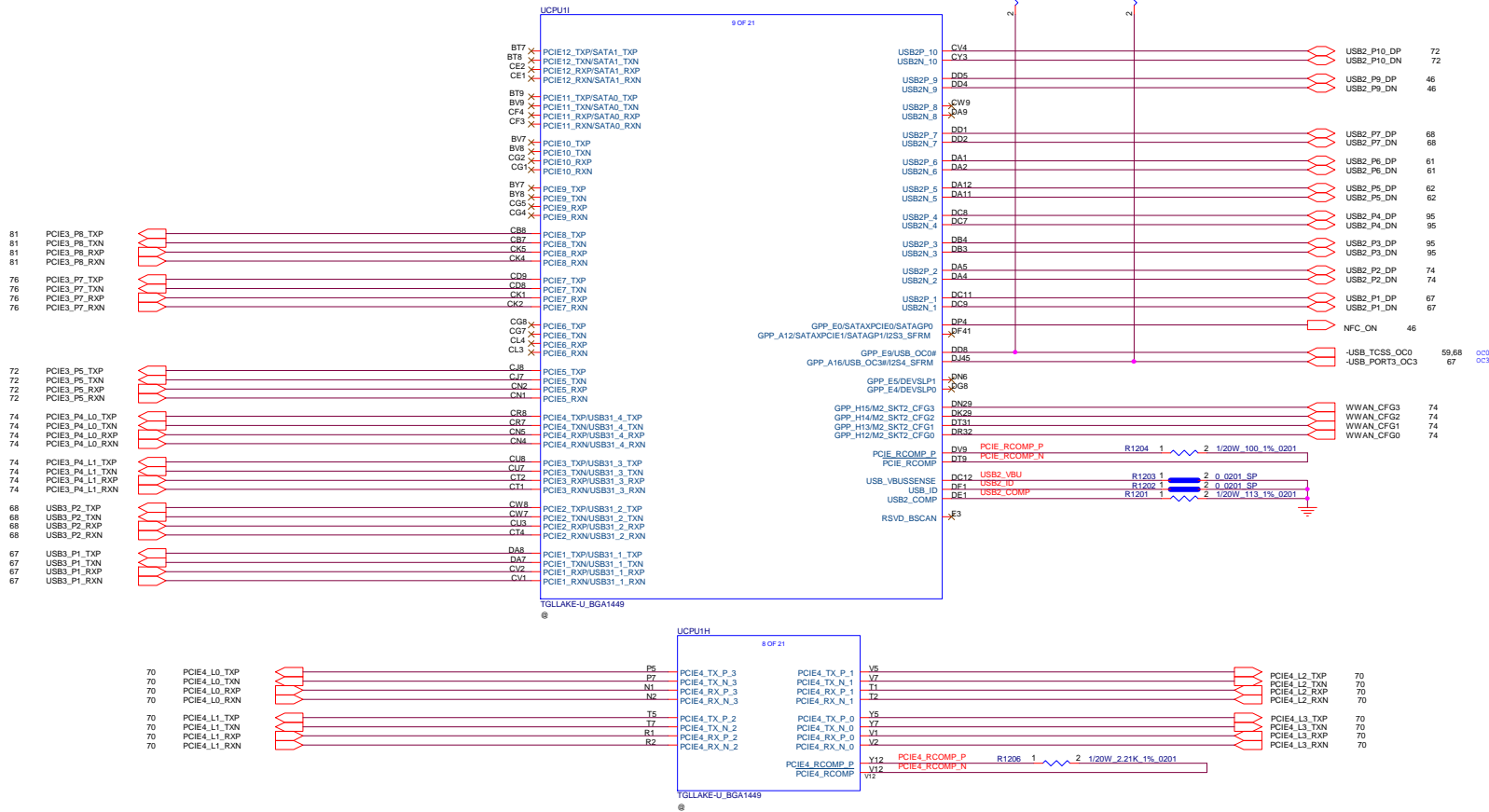
| Flexible I/O Configuration | | | | | | |
|----------------------------|---------------------------|--------|----------|--------------------|--------------------------------|-------------|
| HSIO Port | High Speed Signals | PCI | | HSIO Configuration | Descriptor for PCIe | Net Name |
| | | Device | Function | | | |
| PCH L0 | USB 3.1 #1 / PCIe Gen3 #1 | 1Ch | 0h | USB 3.1 #1 | 1x2, 2x1 Lane Reversal Enabled | USB3_P1 |
| PCH L1 | USB 3.1 #2 / PCIe Gen3 #2 | | 1h | USB 3.1 #2 | | USB3_P2 |
| PCH L2 | USB 3.1 #3 / PCIe Gen3 #3 | | 2h | PCIe Gen3 #3 | | PCIE3_P4_L1 |
| PCH L3 | USB 3.1 #4 / PCIe Gen3 #4 | | 3h | PCIe Gen3 #4 | | PCIE3_P4_L0 |
| PCH L4 | PCIe Gen3 #5 | 1Ch | 4h | PCIe Gen3 #5 | 4x1 Lane Reversal Disabled | PCIE3_P5 |
| PCH L5 | PCIe Gen3 #6 | | 5h | PCIe Gen3 #6 | | N/A |
| PCH L6 | PCIe Gen3 #7 (GbE) | | 6h | PCIe Gen3 #7 (GbE) | | PCIE3_P7 |
| PCH L7 | PCIe Gen3 #8 (GbE) | | 7h | PCIe Gen3 #8 | | PCIE3_P8 |
| PCH L8 | PCIe Gen3 #9 (GbE) | 1Dh | 0h | PCIe Gen3 #9 (x4) | 1x4 Lane Reversal Disabled | N/A |
| PCH L9 | PCIe Gen3 #10 | | 1h | PCIe Gen3 #10 (x4) | | N/A |
| PCH L10 | PCIe Gen3 #11 / SATA #0 | | 2h | PCIe Gen3 #11 (x4) | | N/A |
| PCH L11 | PCIe Gen3 #12 / SATA #1 | | 3h | PCIe Gen3 #12 (x4) | | N/A |
| CPU L0 | PCIe Gen4 x4Lane 0 | 06h | 0h | PCIe Gen4 (x4) L0 | 1x4 Lane Reversal Enabled | PCIE4_L3 |
| CPU L1 | PCIe Gen4 x4Lane 1 | | | PCIe Gen4 (x4) L1 | | PCIE4_L2 |
| CPU L2 | PCIe Gen4 x4Lane 2 | | | PCIe Gen4 (x4) L2 | | PCIE4_L1 |
| CPU L3 | PCIe Gen4 x4Lane 3 | | | PCIe Gen4 (x4) L3 | | PCIE4_L0 |

| PCIe Port Assignment | |
|----------------------|-------------|
| PCIE3_P1 | (USB3_P1) |
| PCIE3_P2 | (USB3_P2) |
| PCIE3_P3 | WWAN Lane 1 |
| PCIE3_P4 | WWAN Lane 0 |
| PCIE3_P5 | (WLAN) |
| PCIE3_P6 | (Reserved) |
| PCIE3_P7 | GbE PHY |
| PCIE3_P8 | (SD Card) |
| PCIE3_P9 (x4) | (dGPU) |
| PCIE4 (x4) | NVMe SSD |

| USB 3.1 Port Assignment | |
|-------------------------|---------------------|
| USB3_P1 | (Type-A Port) (AOU) |
| USB3_P2 | Type-A Port |
| USB3_P3 | (PCIE3_P3) |
| USB3_P4 | (PCIE3_P4) |

| USB 2.0 Port Assignment | |
|-------------------------|------------------------|
| USB2_P1 | (Type-A Port) (AOU) |
| USB2_P2 | WWAN |
| USB2_P3 | Fingerprint Reader |
| USB2_P4 | RGB / IR Hybrid Camera |
| USB2_P5 | Type-C Port B |
| USB2_P6 | Type-C Port C |
| USB2_P7 | Type-A Port |
| USB2_P8 | (Reserve) |
| USB2_P9 | (Smart Card Reader) |
| USB2_P10 | (Bluetooth) |

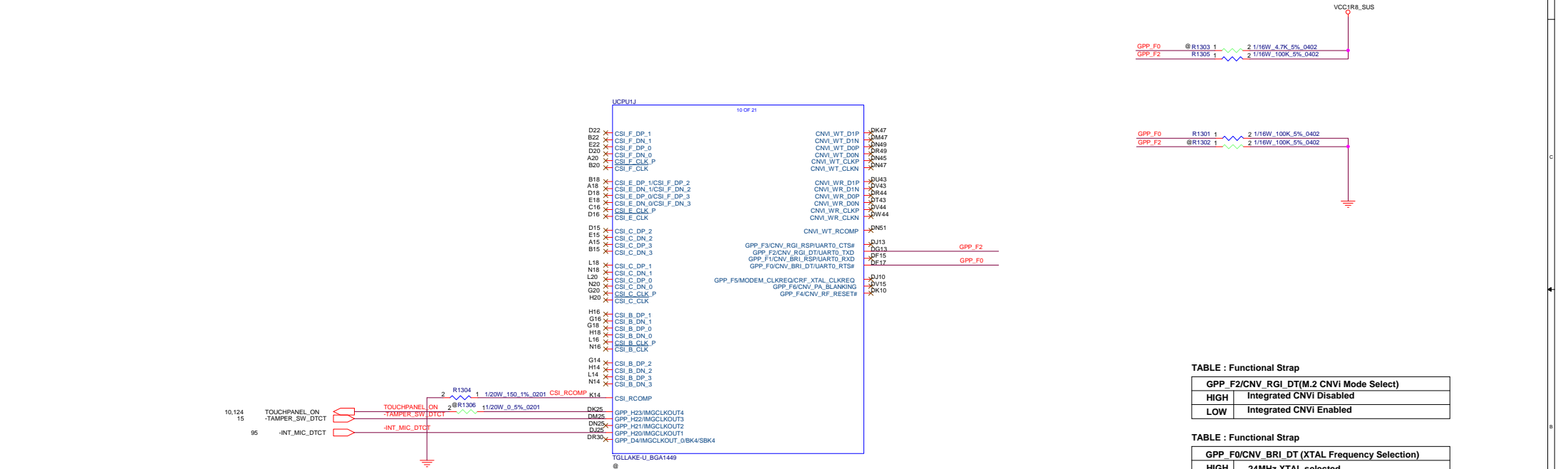
| SATA Port Assignment | |
|----------------------|-------------|
| SATA_P0 | (PCIE3_P11) |
| SATA_P1 | (PCIE3_P12) |



| | |
|---------|------------------------|
| GPP_A11 | SSD_ON |
| GPP_H23 | TOUCHPANEL_ON(Reserve) |
| GPP_D13 | TOUCHPANEL_ON |

VCC3_TOUCHPANEL_ON is connected to both TOUCHPANEL_ON and R_ON via diode.
So, we assume that VCC3_TOUCHPANEL_ON is asserted to "High" by R_ON like attached waveform of VCC3_SSD.
But GPP_H23 is set to low state after reset as PCI GPIO table. Then, VCC3_TOUCHPANEL_ON is not aligned with R_ON like attached waveform.
So we have changed GPIO assignment to GPP_D13 to align power on sequence with R_ON.

| GPIO | Power Well | Voltage Tolerance | Default | Strap | Pin Strap Termination | NMI/SMI Capable | Input Deglitch | Output Power Sequence Deglitch | Pin State During Reset | Pin State Immediately After Reset |
|---------|----------------------------|-------------------|---------|-------|-----------------------|-----------------|----------------|--------------------------------|------------------------|-----------------------------------|
| GPP_A11 | VCCPRIM_1P8 or VCCPRIM_3P3 | 1.8 V or 3.3 V | GP-In | | | no | no | yes(1) | Z | Z |
| GPP_D13 | VCCPRIM_1P8 or VCCPRIM_3P3 | 1.8 V or 3.3 V | GP-In | | | no | no | yes(1) | Z | Z |
| GPP_H23 | VCCPRIM_1P8 or VCCPRIM_3P3 | 1.8 V or 3.3 V | GP-Out | | | no | no | no | Z | L |



| TABLE : Functional Strap | |
|---|--------------------------|
| GPP_F2/CNV_RGI_DT(M.2 CNVi Mode Select) | |
| HIGH | Integrated CNVi Disabled |
| LOW | Integrated CNVi Enabled |

| TABLE : Functional Strap | |
|--|---|
| GPP_F0/CNV_BRI_DT (XTAL Frequency Selection) | |
| HIGH | 24MHz XTAL selected |
| LOW | 38.4MHz XTAL frequency selected (Default) |

[Issue Symptom]
All PCIe device can't recognize

[Root cause]
GPP_F0 strap not correct setting.

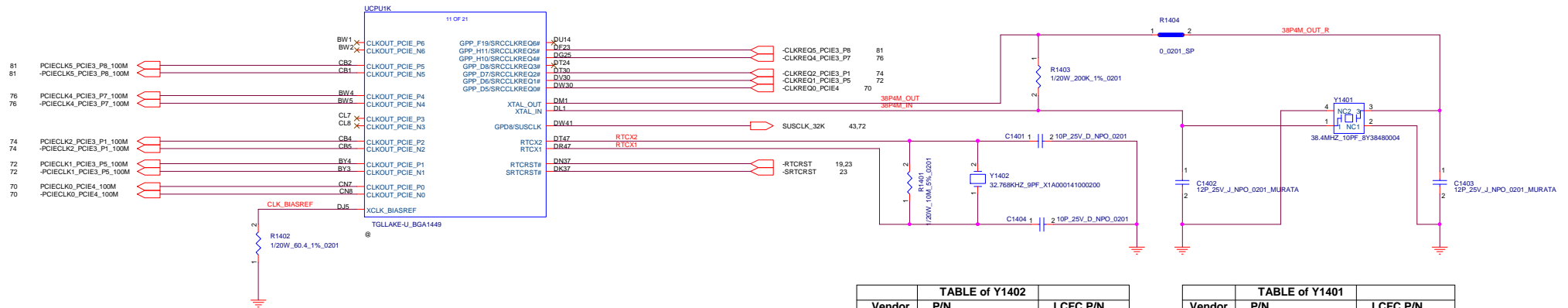
[Solution]
GPIO need to set up "native" and can't have PU resistance.

CNVi_WT_RCOMP

| Interface | Pin Name | Board Rterm (Ohm) | Board DC resistance (ohms) | Main route trace spacing requirement (um) | Notes |
|-----------|---------------|--------------------|----------------------------|---|---|
| CNVi | CNVi_WT_RCOMP | 150Ω ±1% to GND | <0.5 | 200 | This RCOMP can be left unconnected if not used. |

| Lenovo | | | |
|---------------------------------|-------------------|--------------------------------|-----------|
| Project Name : T14s Gen2 | | Title : CPU (9/16): CSI-2/CNVi | |
| Size : C | Document Number : | | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 13 of 130 | |

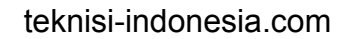
| | | |
|--------|-------------------|------------|
| Port 0 | PCIe Gen4 (x4) | NVMe SSD |
| Port 1 | PCIe Gen3 P5 | (M.2 WLAN) |
| Port 2 | PCIe Gen3 P1 | M.2 WWAN |
| Port 3 | PCIe Gen3 P9 (x4) | (dGPU) |
| Port 4 | PCIe Gen3 P7 | GbE PHY |
| Port 5 | PCIe Gen3 P8 | (SD Card) |
| Port 6 | PCIe Gen3 P6 | (Reserved) |



| | TABLE of Y1402 | |
|--------|-----------------|------------|
| Vendor | P/N | LCFC P/N |
| EPSON | X1A000141000201 | SJ10000IX0 |
| TXC | 9H03280012 | SJ10000J90 |
| KDS | 1TJF090DJ1A000B | SJ10006940 |

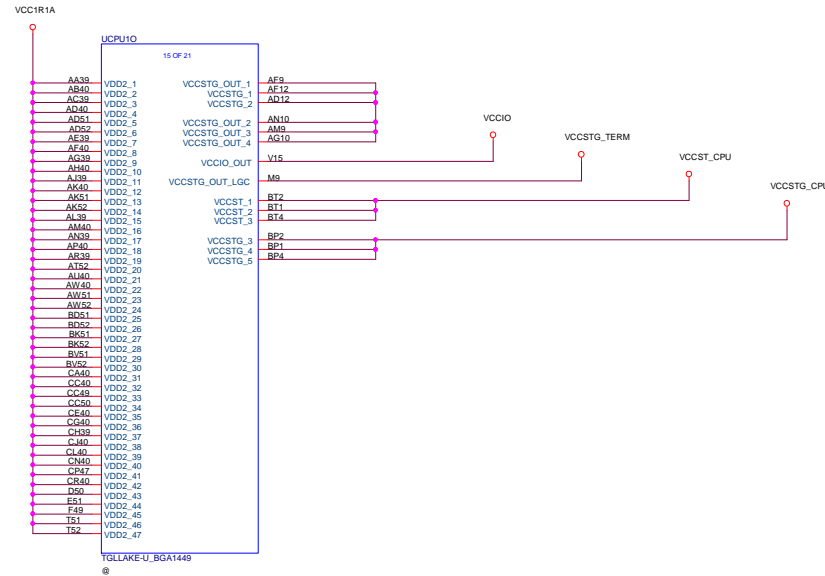
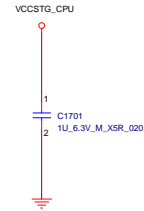
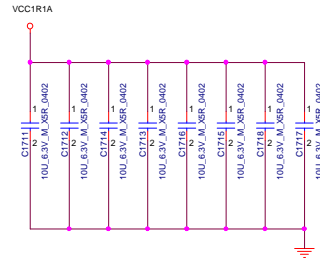
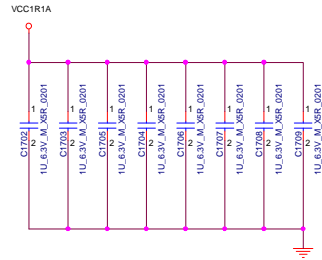
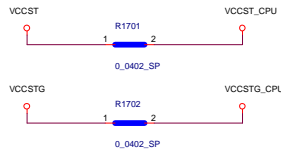
| | | |
|--------|----------------|-------------|
| | TABLE of Y1401 | |
| Vendor | P/N | LCFC P/N |
| TXC | 8Y38480004 | SJ10000SN00 |
| | | |

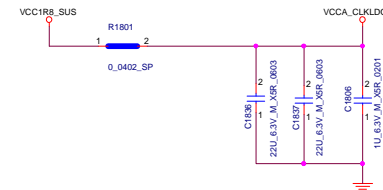
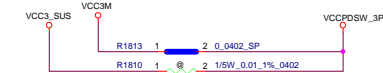
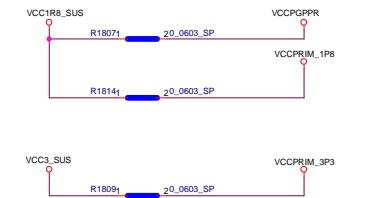
| | | |
|---------|-----------------|-------------|
| TI | SN74LVC1G17DRLR | SA00005MG00 |
| TOSHIBA | TC7SZ17FE | SA00008EZ00 |
| ONSEMI | NL17SZ17XV5T2G | SA00005OU00 |



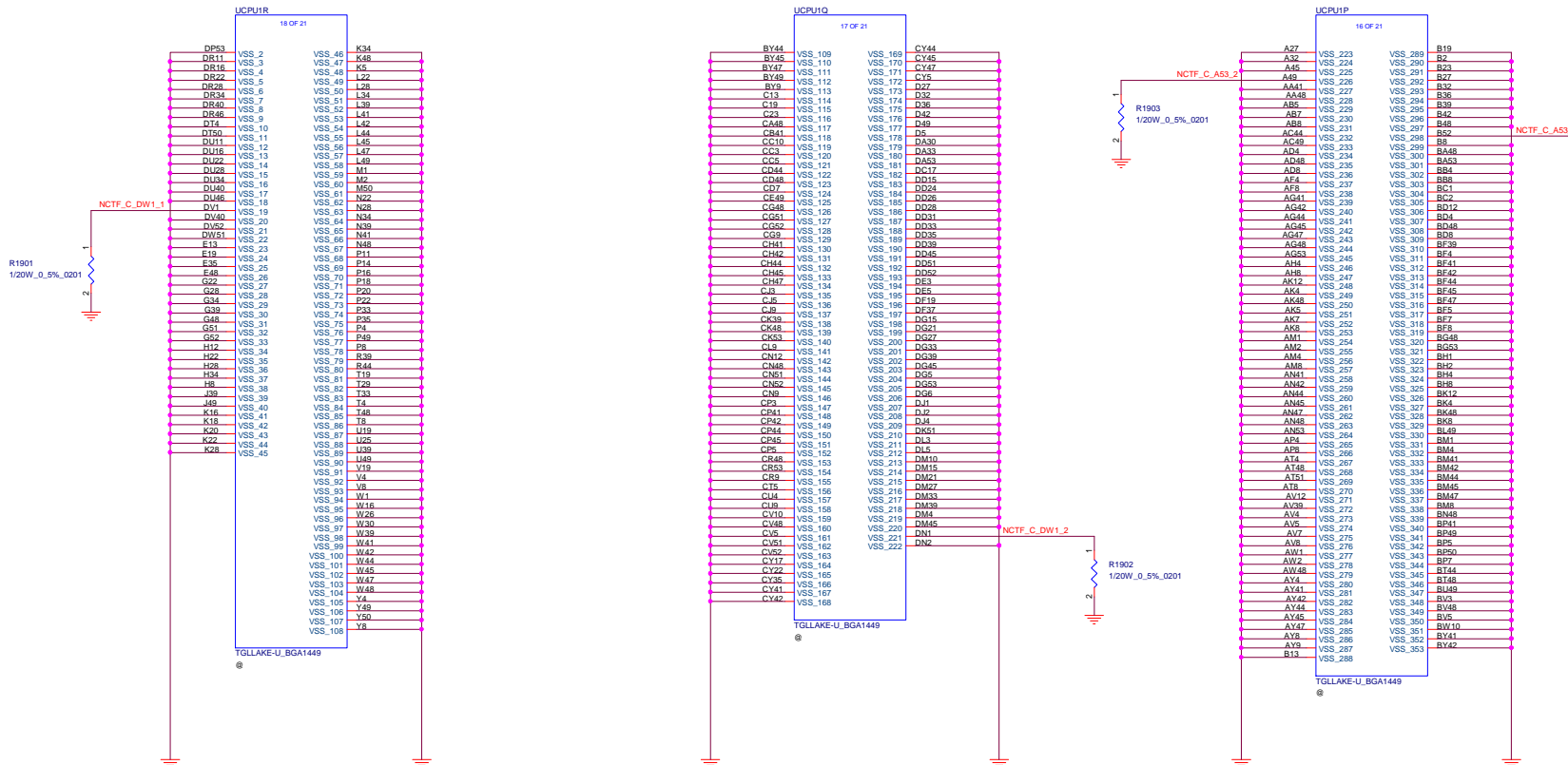
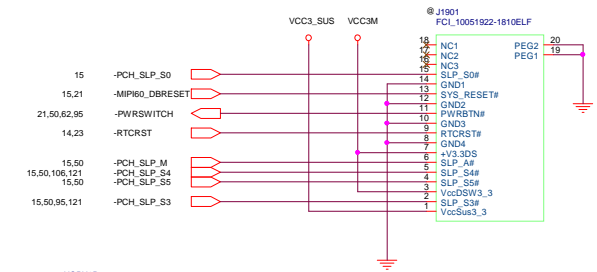
| SPIVCCIOSEL (SPI Operation Voltage Select) | |
|--|---------------------|
| HIGH | SPI Voltage is 1.8V |
| LOW | SPI Voltage is 3.3V |

| GPD7 (Crystal Input Mode) | |
|---------------------------|-------------------------------|
| HIGH | Crystal Input is single ended |
| LOW | Crystal is attached (Default) |





APS/PETS Interface



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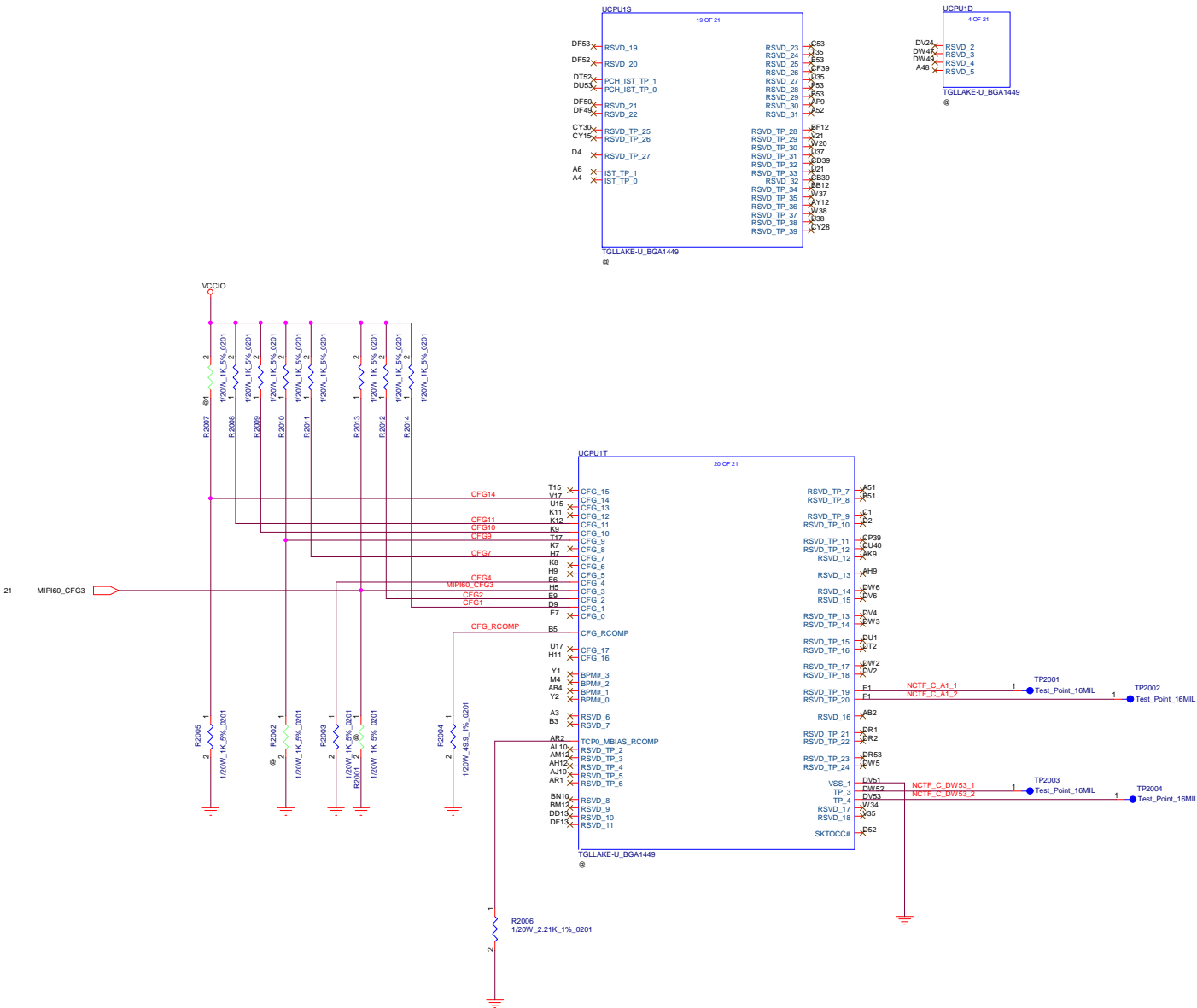
TABLE

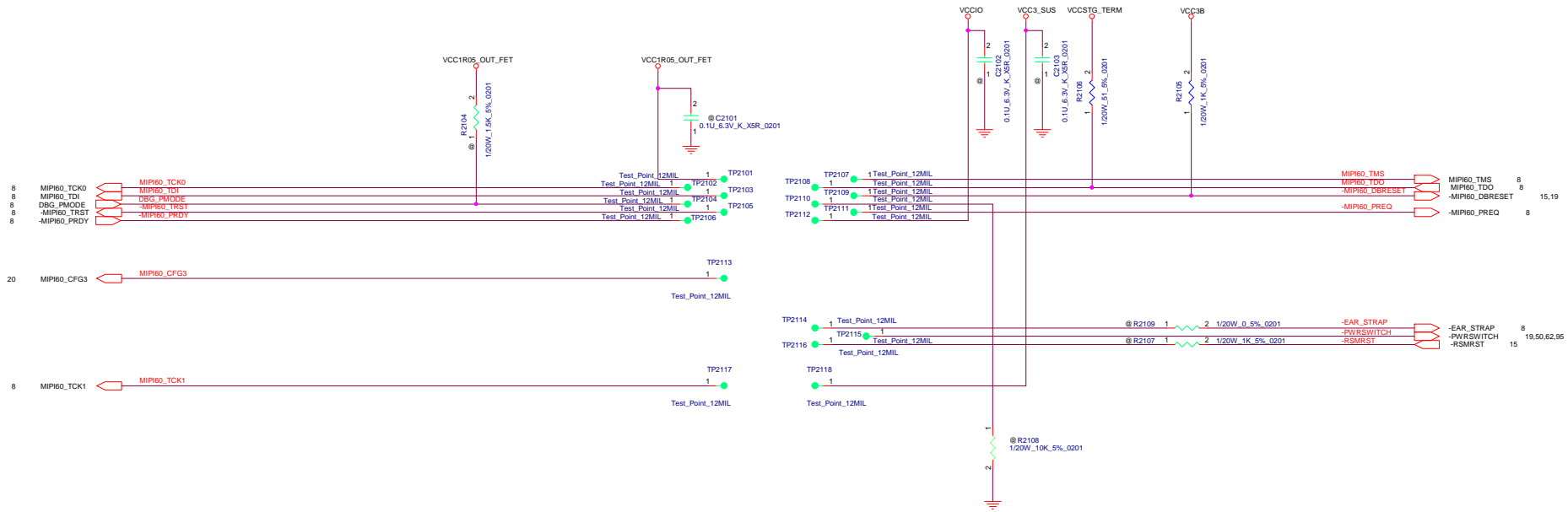
| |
|---------------------------------|
| CFG3: MSR Privacy Bit Feature |
| 1: MSR (C80h) bit[0] setting |
| 0: MSR (C80h) bit[0] overridden |

| |
|------------------|
| CFG4: eDP Enable |
| 1:Disabled |
| 0:Enabled |

| |
|------------------------------|
| CFG9: SVID Bus Communication |
| 1:Enabled |
| 0:Disabled |

| |
|----------------------------|
| CFG14: PEG60 Lane Reversal |
| 1:Normal |
| 0:Reversed |



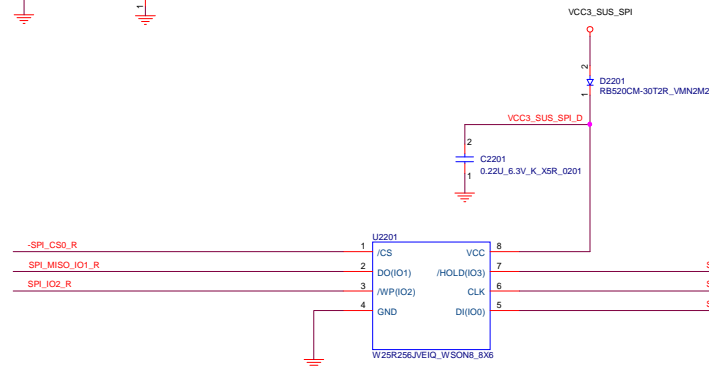


TABLE

| Logic | Ref Des | MIP160 | DC1 2.0 |
|---------|---------|--------|---------|
| Page8 | R0808 | ASM | NO_ASM |
| | R0809 | ASM | NO_ASM |
| Page 20 | R2001 | ASM | NO_ASM |
| Page 22 | J8 | ASM | NO_ASM |
| | C2101 | ASM | NO_ASM |
| | C2102 | ASM | NO_ASM |
| | C2103 | ASM | NO_ASM |
| | R2108 | ASM | NO_ASM |
| | R2106 | ASM | ASM |
| | R2105 | ASM | ASM |
| | R2104 | ASM | NO_ASM |
| | R2107 | ASM | NO_ASM |
| | R2109 | ASM | NO_ASM |

↑
LOGIC

| | |
|---------------------------------|-----------------------------------|
| Lenovo | |
| Project Name : T14s Gen2 | Title : MIP160 DEBUG PORT |
| Size : C | Document Number : Rev : 0.1 |
| Date: Friday, December 18, 2020 | Sheet : 21 of 130 |



| | | |
|--------------------------|------------------|---------------------|
| 32MB (256Mb) 8x6mm WSON8 | | DUAL/QUAD SPI & RPM |
| Winbond | W25R256JVEIQ | SA0000A1Q00 |
| GigaDevice | GD25R256DYIGR | SA0000A1S00 |
| Macronix | MX77L256S0FZ4I42 | SA0000A1R00 |

SIT-R changed as below

TABLE:U2201

| | | |
|--------------------------|------------------|---------------------|
| 32MB (256Mb) 8x6mm WSON8 | | DUAL/QUAD SPI & RPM |
| Winbond | W25R256JVEIN | SA0000BND00 |
| GigaDevice | GD25R256DY1GR | SA0000A1S00 |
| Macronix | MX77L25650FZ4142 | SA0000A1R00 |

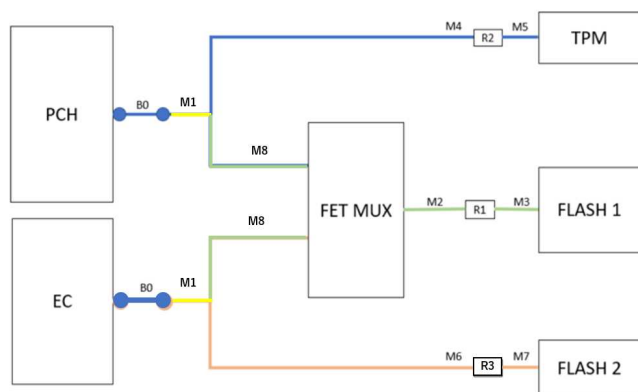


TABLE:JBIOS

| | |
|-----------------------|----------------|
| WSO8 SPI FLASH SOCKET | |
| ACES | 50950-0084N-00 |
| | |

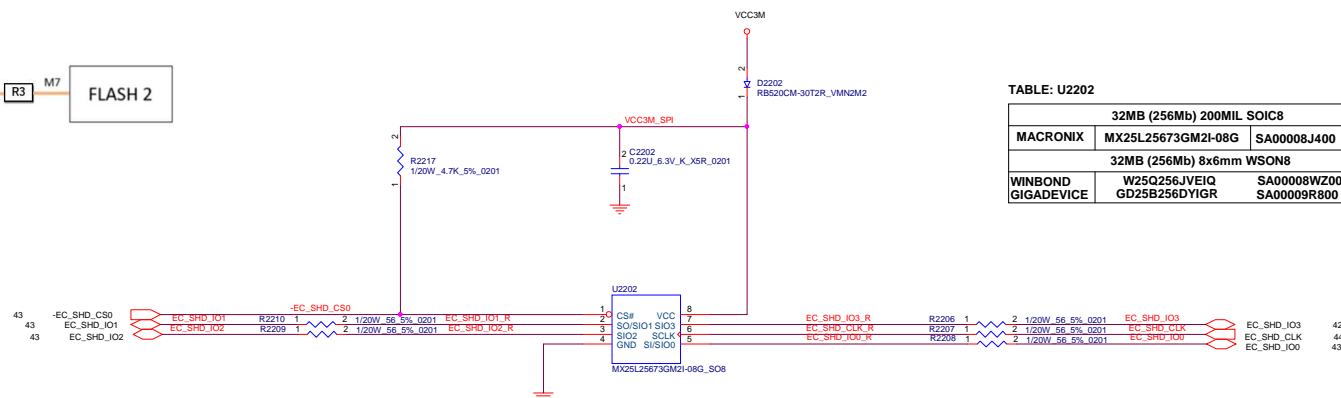


TABLE: U2202

| | | |
|---------------------------|------------------------------|------------------------|
| 32MB (256Mb) 200MIL SOIC8 | | |
| MACRONIX | MX25L25673GM2I-08G | SA00008J40 |
| 32MB (256Mb) 8x6mm WSON8 | | |
| WINBOND GIGADEVICE | W25Q256JVEI GD25B256DYIGR | SA00008WZ SA00009R8 |

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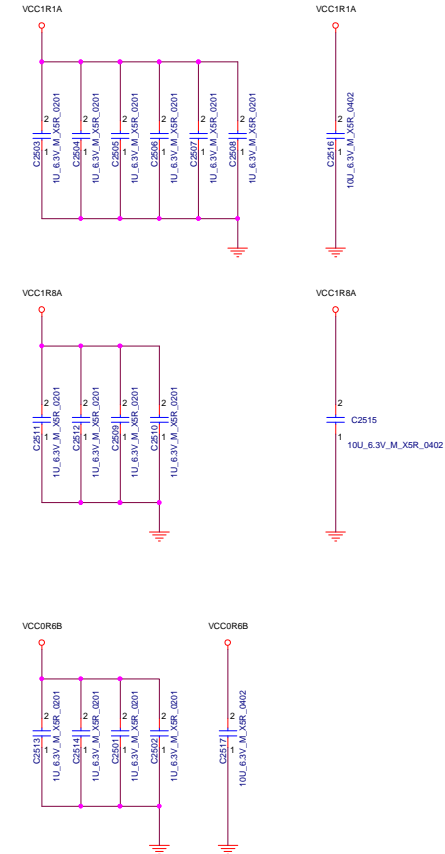
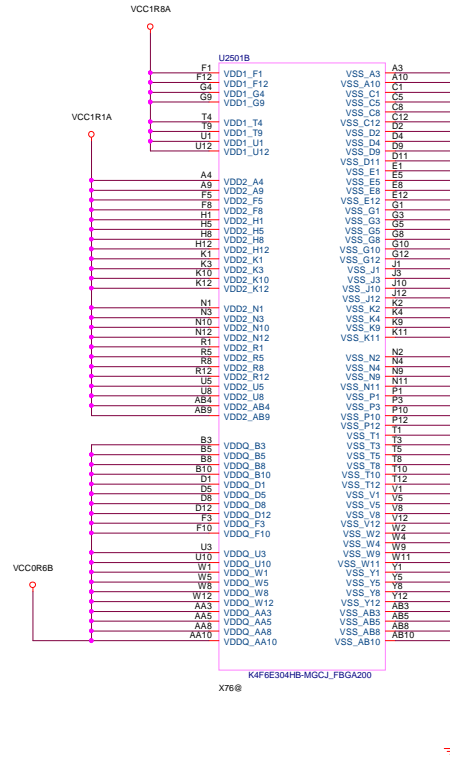
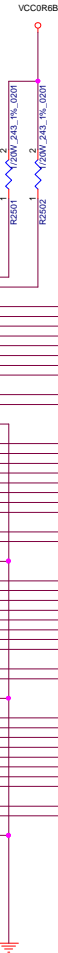
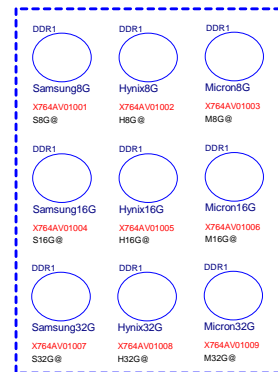


TABLE : LPDDR4x Source

| Supplier | Capacity | Supplier's P/N | Package Size? | | Die? | Device Configuration? | Memory |
|----------|----------|--------------------------|----------------|-----|--------------------|---------------------------|--------|
| SK Hynix | 16Gb | H9HCNNNBKMLXLR-NEE | 10.0 x 15.0 mm | DDP | 8Gb (512Mx16x1Ch) | 1 Rank x (512Mx16) x 2 Ch | 8GB |
| | 32Gb | H9HCNNNPCMFLXLR-NEE | 10.0 x 15.0 mm | QDP | 8Gb (512Mx16x1Ch) | 2 Rank x (512Mx16) x 2 Ch | 16GB |
| | 64Gb | H9HCNNNFAMMLXLR-NEE | 10.0 x 15.0 mm | ODP | 8Gb (1Gx8x1Ch) | 2 Rank x (1Gx16) x 2 Ch | 32GB |
| | 16Gb | K4UE3S4AA-MGCR | 10.0 x 15.0 mm | SDP | 16Gb (512Mx16x2Ch) | 1 Rank x (512Mx16) x 2 Ch | 8GB |
| Samsung | 32Gb | K4UE3D4AA-MGCR | 10.0 x 15.0 mm | DDP | 16Gb (512Mx16x2Ch) | 2 Rank x (512Mx16) x 2 Ch | 16GB |
| | 64Gb | K4UCE3Q4AA-MGCR | 10.0 x 15.0 mm | QDP | 16Gb (T.B.D) | 2 Rank x (1Gx16) x 2 Ch | 32GB |
| | 16Gb | MT53E512M32D2NP-046 WT:E | 10.0 x 14.5 mm | DDP | 8Gb (512Mx16x1Ch) | 1 Rank x (512Mx16) x 2 Ch | 8GB |
| | 32Gb | MT53E1G32D2NP-046 WT:A | 10.0 x 14.5 mm | DDP | 16Gb (T.B.D) | 2 Rank x (512Mx16) x 2 Ch | 16GB |
| Micron | 64Gb | MT53E2G32D4NQ-046 WT:A | 10.0 x 14.5 mm | QDP | 16Gb (T.B.D) | 2 Rank x (1Gx16) x 2 Ch | 32GB |

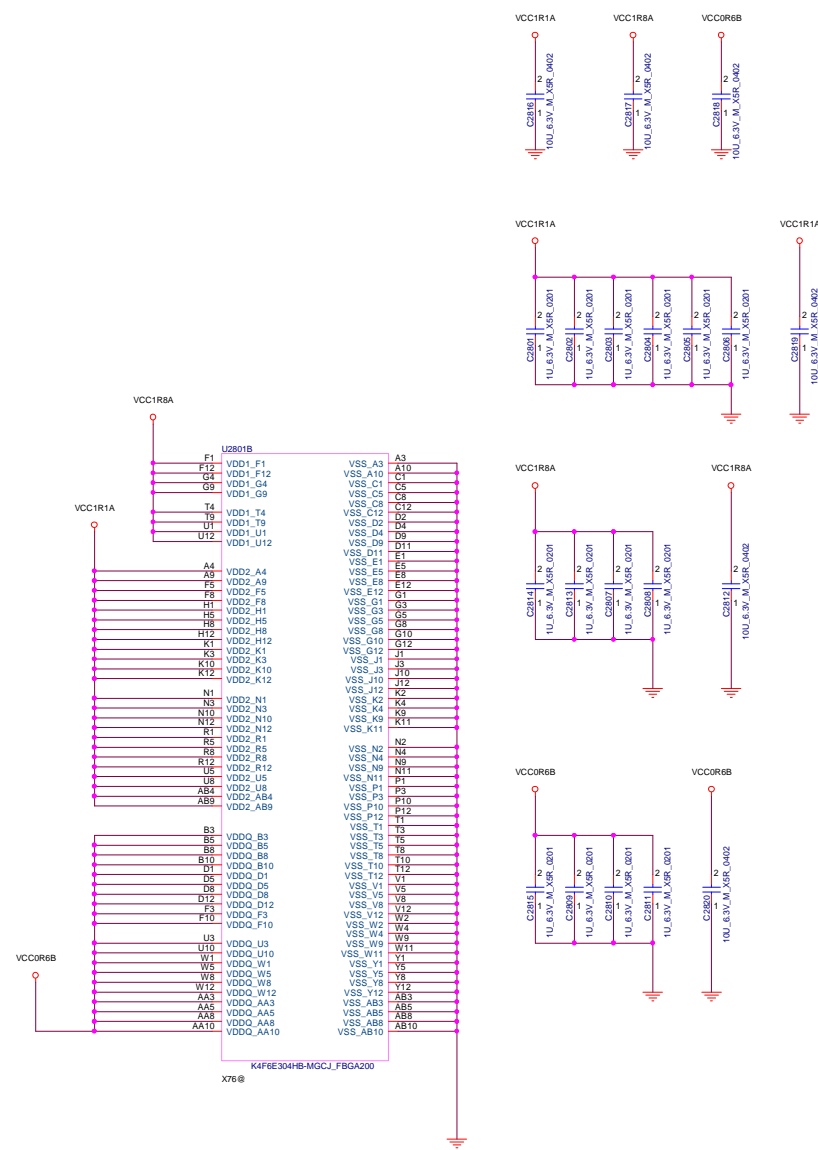
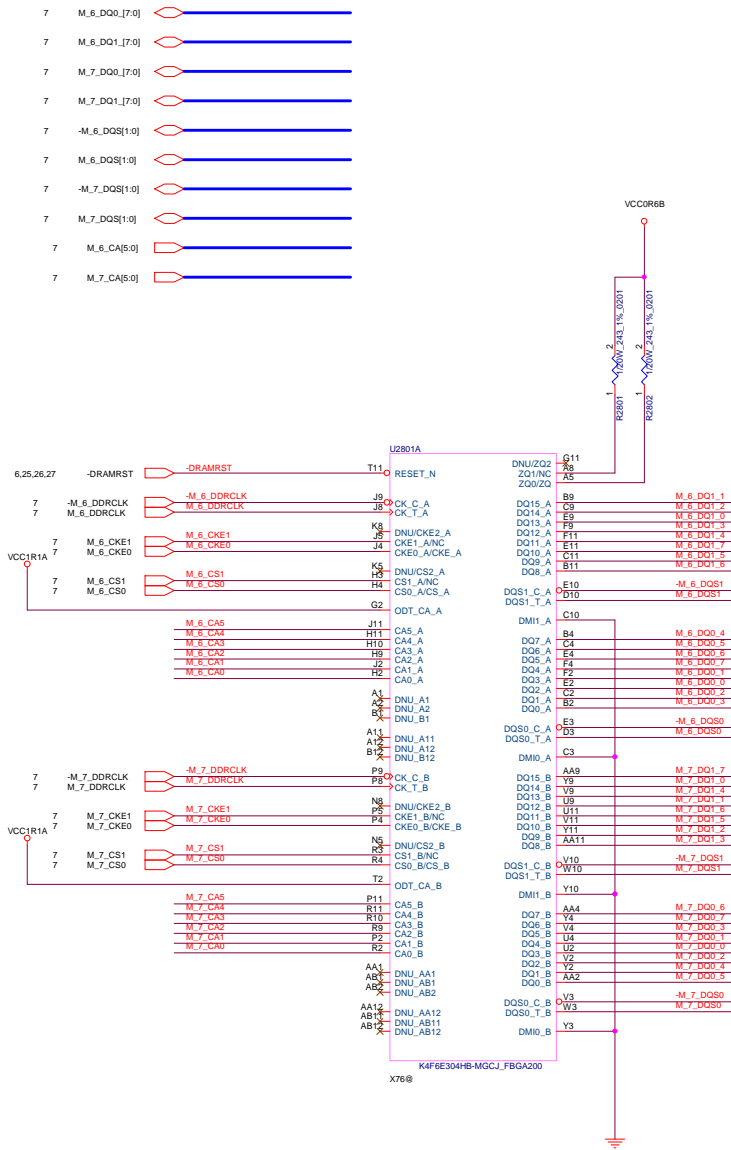



TABLE : LPDDR4x Source

| Supplier | Capacity | Supplier's P/N | Package Size? | Die? | Device Configuration? | Memory |
|----------|----------|--------------------------|----------------|------|-----------------------|---------------------------|
| SK Hynix | 16Gb | H9HCNNNBKMLXR-NEE | 10.0 x 15.0 mm | DDP | 8Gb (512Mx16x1Ch) | 1 Rank x (512Mx16) x 2 Ch |
| | 32Gb | H9HCNNNCPMLXR-NEE | 10.0 x 15.0 mm | QDP | 8Gb (512Mx16x1Ch) | 2 Rank x (512Mx16) x 2 Ch |
| | 64Gb | H9HCNNNFAMMLXR-NEE | 10.0 x 15.0 mm | ODP | 8Gb (1Gx8x1Ch) | 2 Rank x (1Gx16) x 2 Ch |
| Samsung | 16Gb | K4U6E3S4AA-MGCR | 10.0 x 15.0 mm | SDP | 16Gb (512Mx16x2Ch) | 1 Rank x (512Mx16) x 2 Ch |
| | 32Gb | K4UBE3D4AA-MGCR | 10.0 x 15.0 mm | DDP | 16Gb (512Mx16x2Ch) | 2 Rank x (512Mx16) x 2 Ch |
| | 64Gb | K4UCE3Q4AA-MGCR | 10.0 x 15.0 mm | QDP | 16Gb (T.B.D) | 2 Rank x (1Gx16) x 2 Ch |
| Micron | 16Gb | MT53E512M32D2NP-046 WT:E | 10.0 x 14.5 mm | DDP | 8Gb (512Mx16x1Ch) | 1 Rank x (512Mx16) x 2 Ch |
| | 32Gb | MT53E1G32D2NP-046 WT:A | 10.0 x 14.5 mm | DDP | 16Gb (T.B.D) | 2 Rank x (512Mx16) x 2 Ch |
| | 64Gb | MT53E2G32D4NQ-046 WT:A | 10.0 x 14.5 mm | QDP | 16Gb (T.B.D) | 2 Rank x (1Gx16) x 2 Ch |

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| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : PWR SW/PEN CHARGER INTERFACE |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 29 of 130 |

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|---|-------------------|---------------------------|
|  | | |
| Project Name : T14s Gen2 | | Title : HDMI CONNECTOR |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 30 of 130 |

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|---|-------------------|--|
|  | | |
| Project Name : T14s Gen2 | | Title : THUNDERBOLT RETIMER B (1/2) |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 31 of 130 |

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|---|-------------------|--|
|  | | |
| Project Name : T14s Gen2 | | Title : THUNDERBOLT RETIMER B (2/2) |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 32 of 130 |


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|  | | |
| Project Name : T14s Gen2 | | Title : THUNDERBOLT RETIMER C (1/2) |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 33 of 130 |

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|---------------------------------|-------------------|--|
| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : THUNDERBOLT RETIMER C (2/2) |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 34 of 130 |

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|---|-------------------|------------------------------|
|  | | |
| Project Name : T14s Gen2 | | Title : USB PD CONTROLLER |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 35 of 130 |

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|---------------------------------|-------------------|----------------------------------|
| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : THUNDERBOLT CONNECTOR |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 37 of 130 |

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| | | |
|---------------------------------|-------------------|---------------------------------|
| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : USB TYPE-A CONNECTOR |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 38 of 130 |

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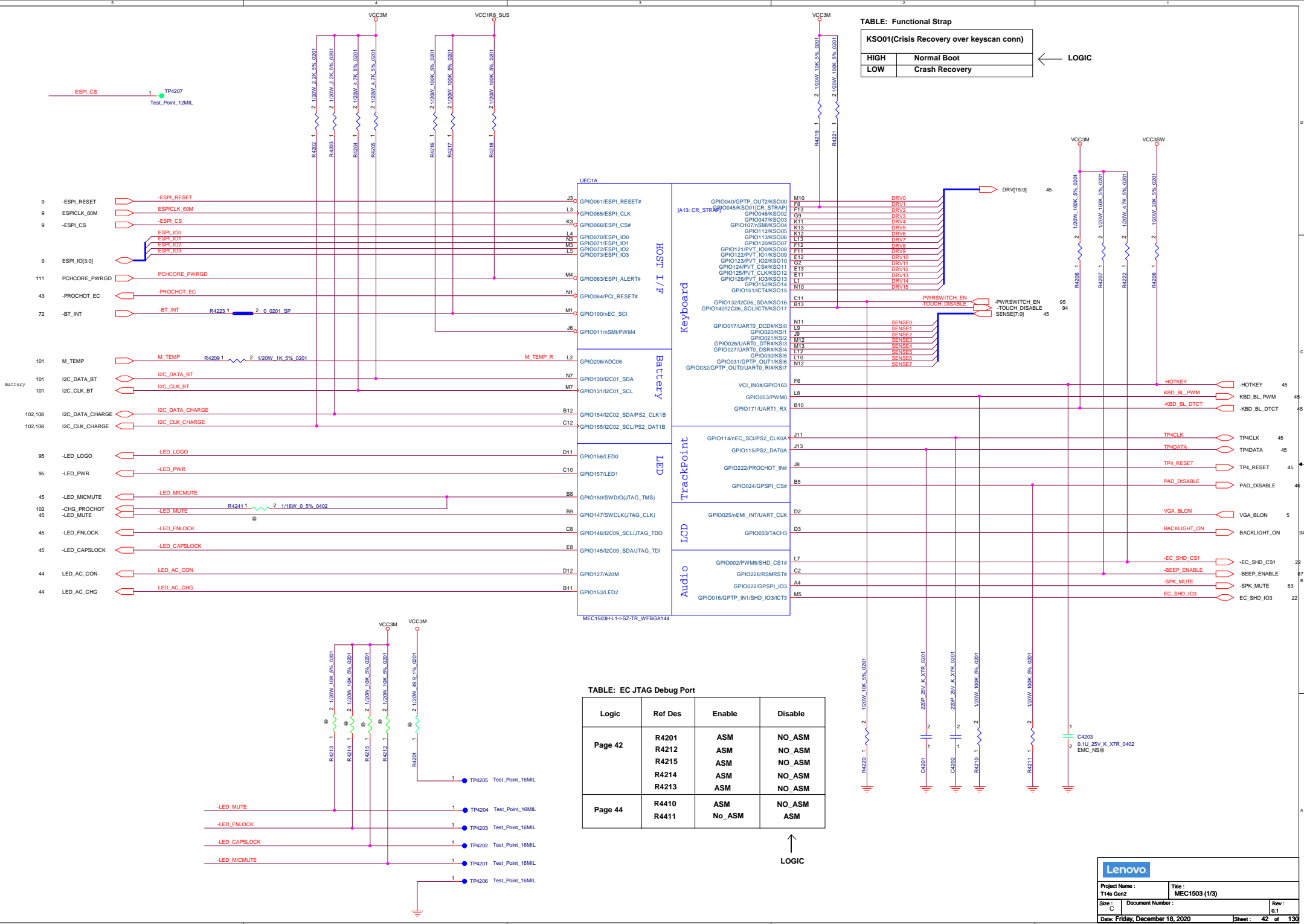
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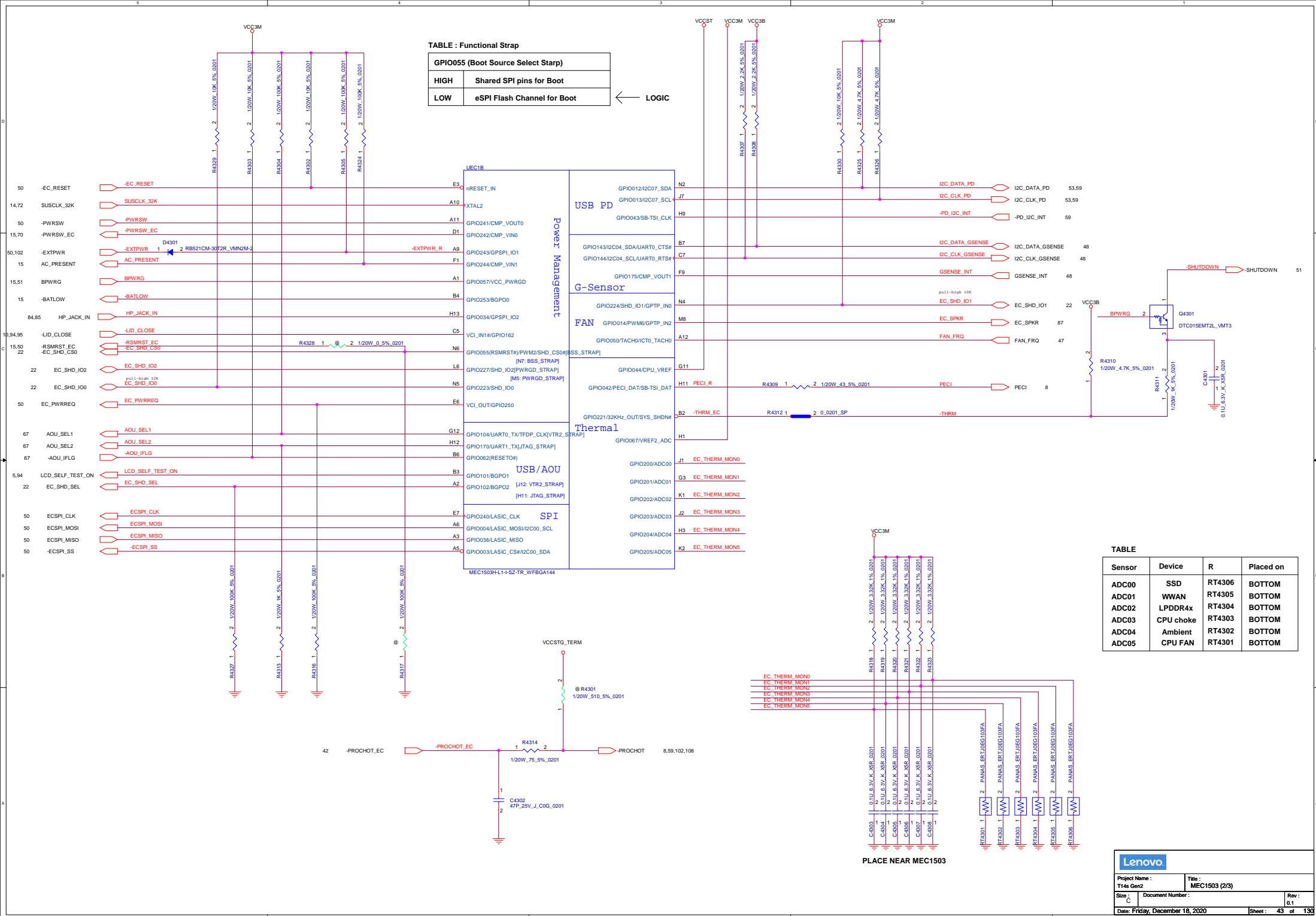
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|--------------------|---------------------------|-----------------|
| Title | | |
| <Title> | | |
| Size | Document Number | Rev |
| Custom? (is Desc?) | | 0.1 |
| Date: | Friday, December 18, 2020 | Sheet 39 of 130 |

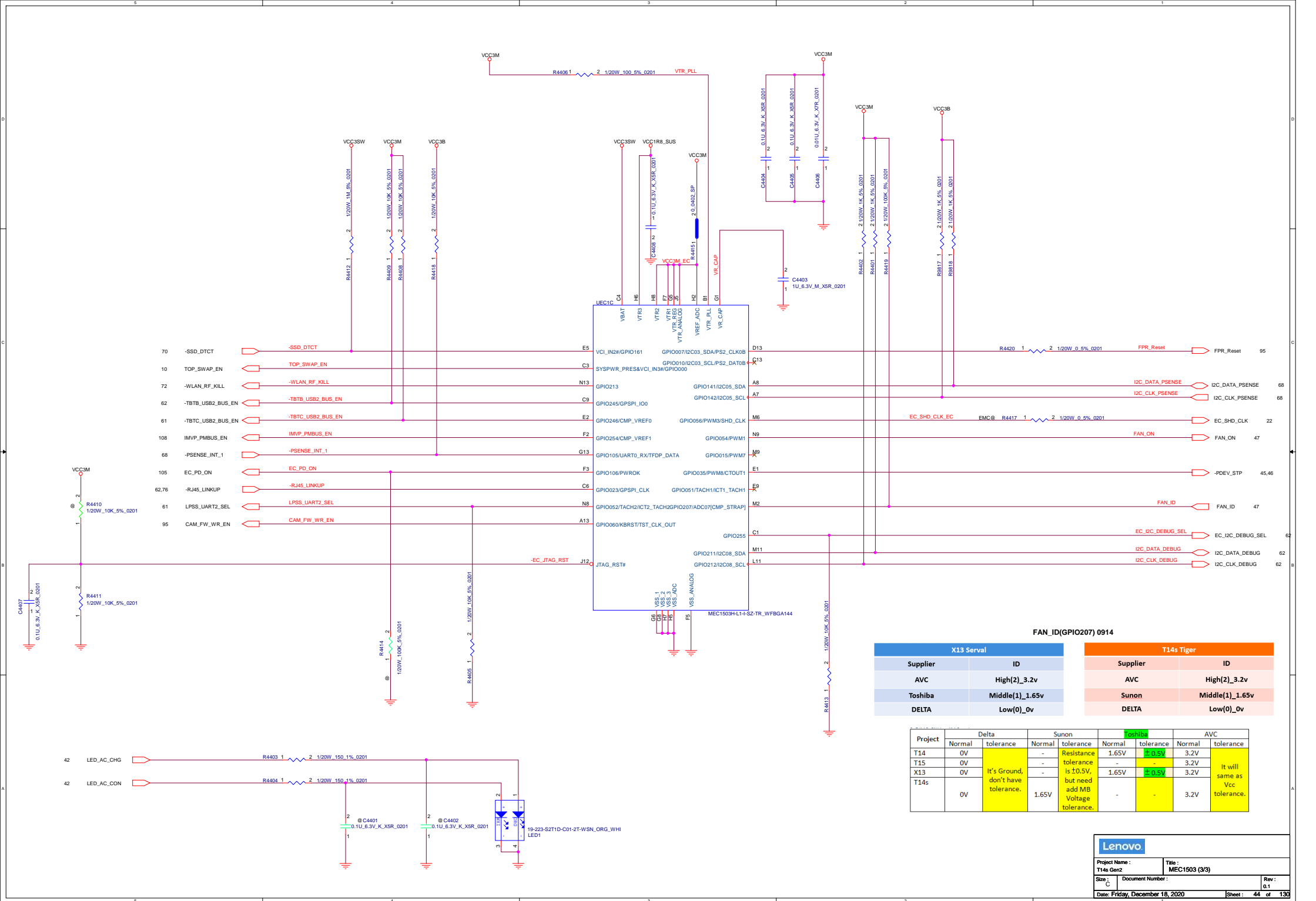
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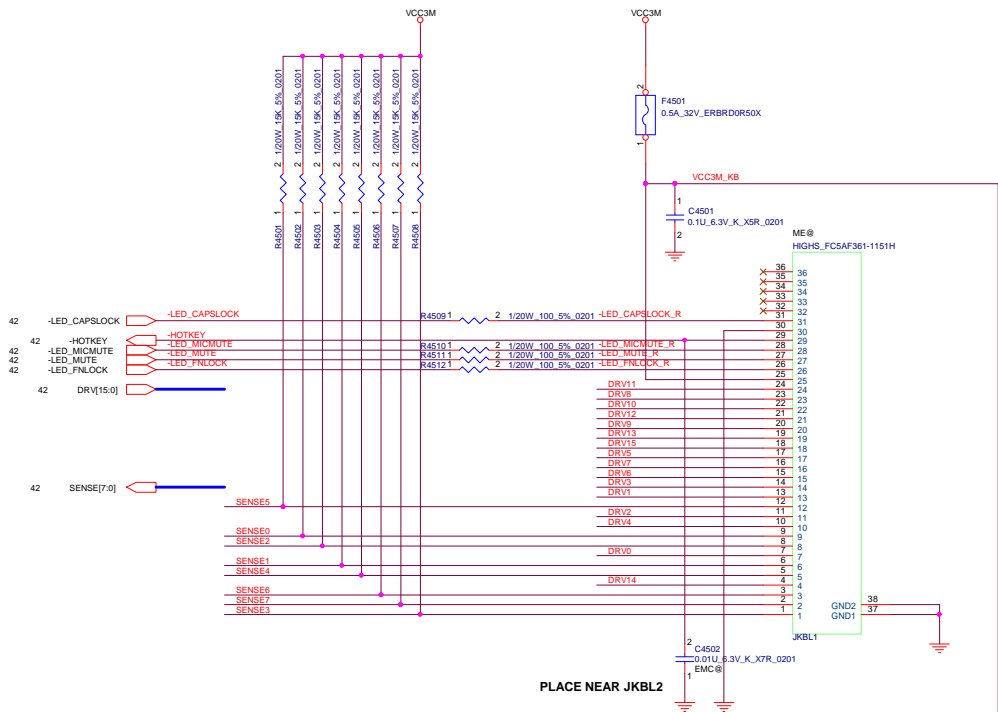
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| Project Name : T14s Gen2 | | Title : BLANK |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 41 of 130 |

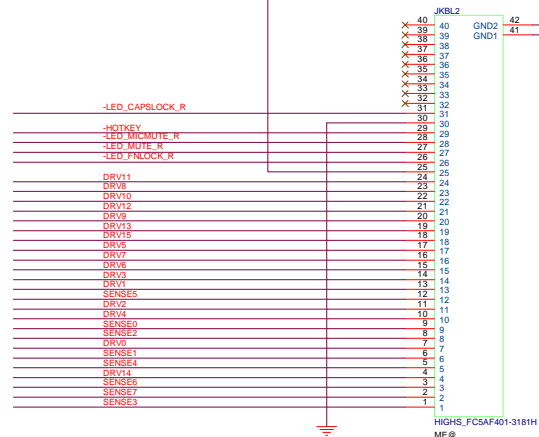




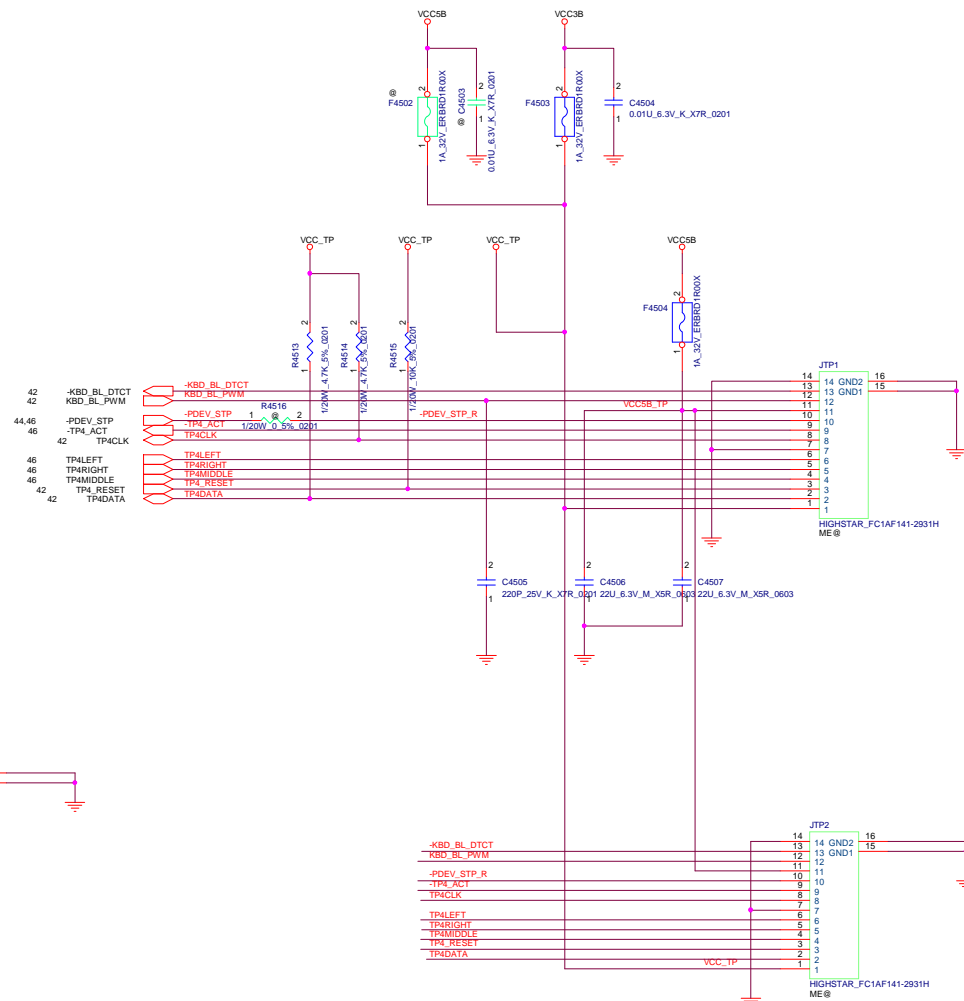




PLACE NEAR JKBL2



JKBL1(36Pin) & JTP1: Serval_X13 => Top side
 JKBL2(40Pin) & JTP2: Tiger_T14s => Bot side (CPU)
 SIT check 0921



Matrix Mapping and Membrane/TrackPoint FPC Pin Assign

| Sense (S1 ~ S8) | Membrane Pin Assignment | TrackPoint and Backlight FPC Pin Assignment | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-------------------------|---|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|--|-----|--------|---|--------|---|----------|---|-----------|---|---------|---|---------|---|----------|---|-----------|---|------------|---|-----------|----|----------|--|-----|--------|---|--------|---|----------|---|-----------|---|---------|---|---------|---|----------|---|-----------|---|------------|---|-----------|----|----------|
| <table border="1"> <tr><th>Pin</th><th>Signal</th></tr> <tr><td>1</td><td>S1</td></tr> <tr><td>2</td><td>S2</td></tr> <tr><td>3</td><td>S3</td></tr> <tr><td>4</td><td>S4</td></tr> <tr><td>5</td><td>S5</td></tr> <tr><td>6</td><td>S6</td></tr> <tr><td>7</td><td>S7</td></tr> <tr><td>8</td><td>S8</td></tr> </table> | Pin | Signal | 1 | S1 | 2 | S2 | 3 | S3 | 4 | S4 | 5 | S5 | 6 | S6 | 7 | S7 | 8 | S8 | <table border="1"> <tr><th>Pin</th><th>Signal</th></tr> <tr><td>1</td><td>VCC3V3</td></tr> <tr><td>2</td><td>TP4 DATA</td></tr> <tr><td>3</td><td>TP4 RESET</td></tr> <tr><td>4</td><td>TP4 ACT</td></tr> <tr><td>5</td><td>TP4 CLK</td></tr> <tr><td>6</td><td>TP4 LEFT</td></tr> <tr><td>7</td><td>TP4 RIGHT</td></tr> <tr><td>8</td><td>TP4 MIDDLE</td></tr> <tr><td>9</td><td>TP4 RESET</td></tr> <tr><td>10</td><td>TP4 DATA</td></tr> </table> | Pin | Signal | 1 | VCC3V3 | 2 | TP4 DATA | 3 | TP4 RESET | 4 | TP4 ACT | 5 | TP4 CLK | 6 | TP4 LEFT | 7 | TP4 RIGHT | 8 | TP4 MIDDLE | 9 | TP4 RESET | 10 | TP4 DATA | <table border="1"> <tr><th>Pin</th><th>Signal</th></tr> <tr><td>1</td><td>VCC3V3</td></tr> <tr><td>2</td><td>TP4 DATA</td></tr> <tr><td>3</td><td>TP4 RESET</td></tr> <tr><td>4</td><td>TP4 ACT</td></tr> <tr><td>5</td><td>TP4 CLK</td></tr> <tr><td>6</td><td>TP4 LEFT</td></tr> <tr><td>7</td><td>TP4 RIGHT</td></tr> <tr><td>8</td><td>TP4 MIDDLE</td></tr> <tr><td>9</td><td>TP4 RESET</td></tr> <tr><td>10</td><td>TP4 DATA</td></tr> </table> | Pin | Signal | 1 | VCC3V3 | 2 | TP4 DATA | 3 | TP4 RESET | 4 | TP4 ACT | 5 | TP4 CLK | 6 | TP4 LEFT | 7 | TP4 RIGHT | 8 | TP4 MIDDLE | 9 | TP4 RESET | 10 | TP4 DATA |
| Pin | Signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | S1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | S2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | S3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | S4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | S5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | S6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | S7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | S8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Pin | Signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | VCC3V3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | TP4 DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | TP4 RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | TP4 ACT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | TP4 CLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | TP4 LEFT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | TP4 RIGHT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | TP4 MIDDLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | TP4 RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | TP4 DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Pin | Signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | VCC3V3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | TP4 DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | TP4 RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | TP4 ACT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | TP4 CLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | TP4 LEFT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | TP4 RIGHT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | TP4 MIDDLE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | TP4 RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | TP4 DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

This matrix has some unnecessary mappings (e.g. 125, E22, etc.) due to universal use purpose.

For NFC

For Smart card


For Clickpad

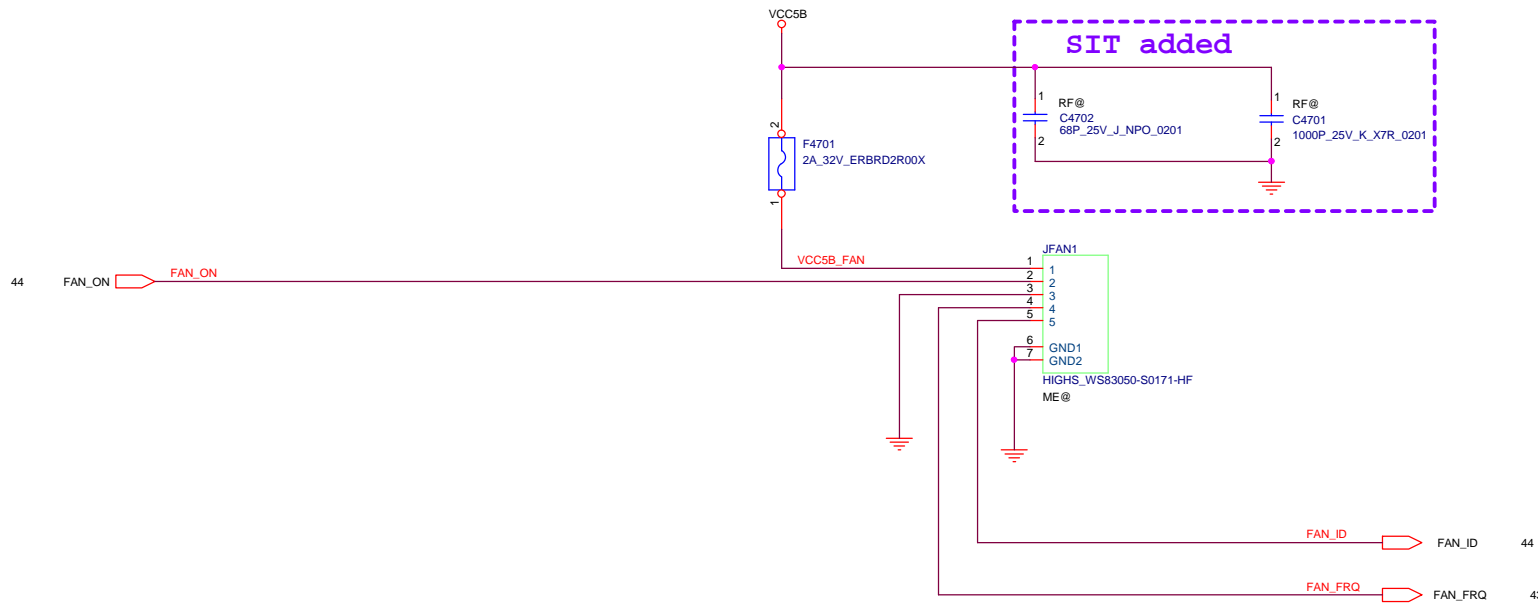


For NFC 05/09 OK

For Clickpad 05/09 OK

For Smart card 05/09 OK

| | | | |
|---|-------------------|-------------------------------------|-----------|
|  | | | |
| Project Name : T14s Gen2 | | Title : TOUCH PAD/Smart card/NFC | |
| Size : | Document Number : | Rev : 0.1 | |
| Date: Friday, December 18, 2020 | | Sheet : | 46 of 130 |



| Pin No. | Signal | Note | Color |
|---------|--------|----------|-------|
| 1 | VCC | +5V | Black |
| 2 | PWM | PWM | Black |
| 3 | GND | — | Black |
| 4 | FG | 2 Pulses | Black |
| 5 | ID | Fan ID | Black |
| --- | --- | --- | --- |

PIN1:+
PIN2:PWM
PIN3:-
PIN4:FG
PIN5:ID

| | | | | | |
|--|------------|------------------------------|------------|----------------|------------------------------|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2018/01/12 | Deciphered Date | 2018/01/12 | FAN CONNECTOR | |
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| | | | | Date: | Friday, December 18, 2020 |
| | | | | Sheet | 47 of 130 |
| | | | | Rev | 0.1 |

TABLE : U4801

| P/N | ADDR_SEL | Address |
|------------|----------|--|
| LIS2DWLTR | H L | 32h (W) & 33h (R) 30h (W) & 31h (R) |
| KX022-1020 | H L | 3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R) |
| BMA280 | H L | 32h (W) & 33h (R) 30h (W) & 31h (R) |

ST and Bosch I2C address is same but can be identified by Chip_ID

TABLE of G-Sensor (U4801)

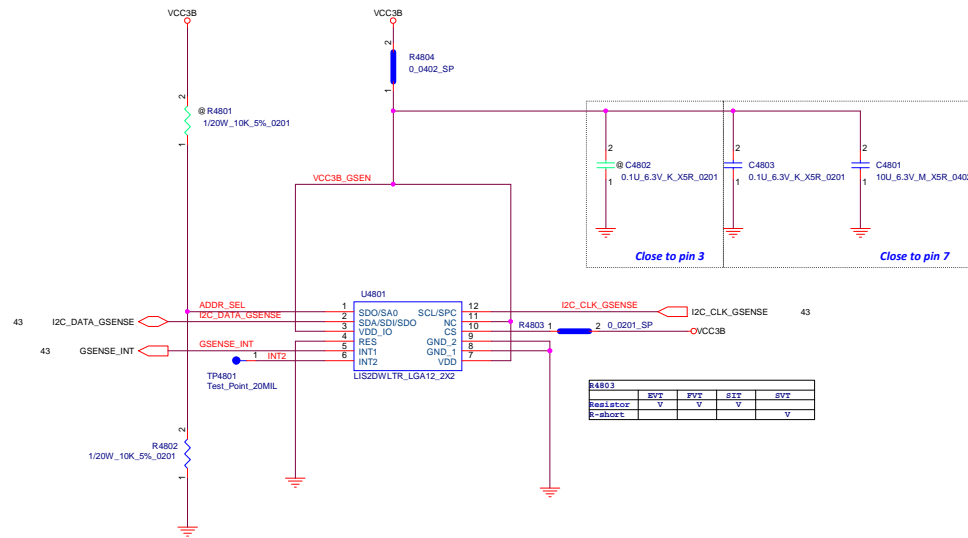
| Vendor | P/N | LCFC P/N |
|--------|------------|-------------|
| ST | LIS2DWLTR | SA00009AQ00 |
| Kionix | KX022-1020 | SA000081E00 |
| BOSCH | BMA280 | SA0000A1600 |

Table 2. Pin description


| Pin# | Name | Function |
|------|-------------------|--|
| 1 | SDO SA0 | SPI serial data output (SDO) I ² C less significant bit of the device address (SA0) |
| 2 | SDA SDI SDO | I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO) |
| 3 | Vdd_IO | Power supply for I/O pins |
| 4 | RES | Connect to GND |
| 5 | INT1 | Interrupt pin 1 |
| 6 | INT2 | Interrupt pin 2 |
| 7 | Vdd | Power supply |
| 8 | GND | 0 V supply |
| 9 | GND | 0 V supply |
| 10 | CS | SPI enable I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled) |
| 11 | NC | Internally not connected. Can be tied to VDD, VDDIO, or GND. |
| 12 | SCL SPC | I ² C serial clock (SCL) SPI serial port clock (SPC) |

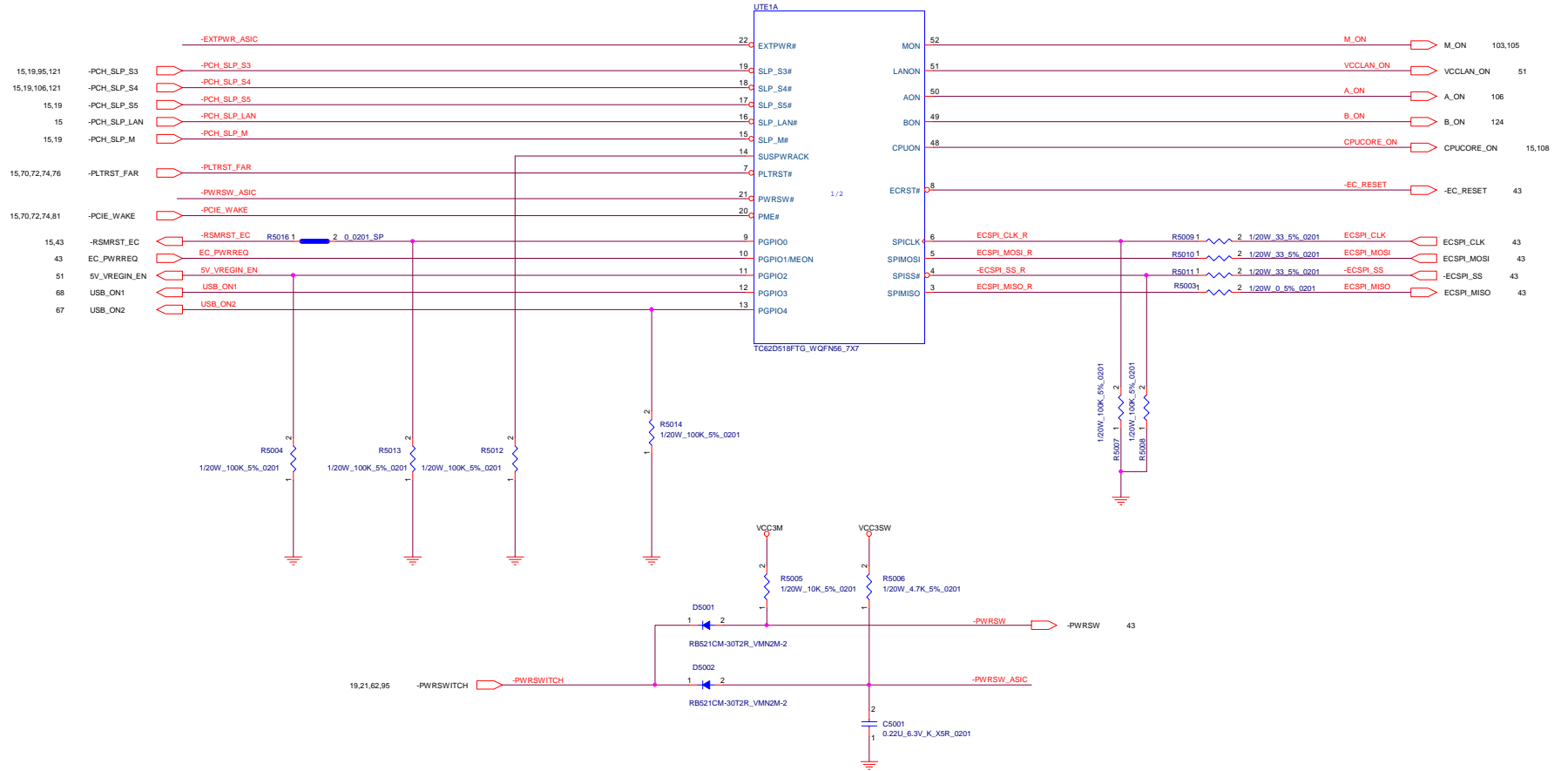
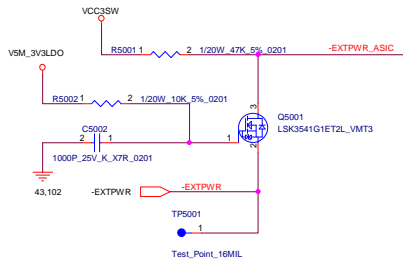
TABLE : G-Sensor Power

| | |
|-------------|-------|
| HDD Support | VCC3M |
| SSD Only | VCC3B |



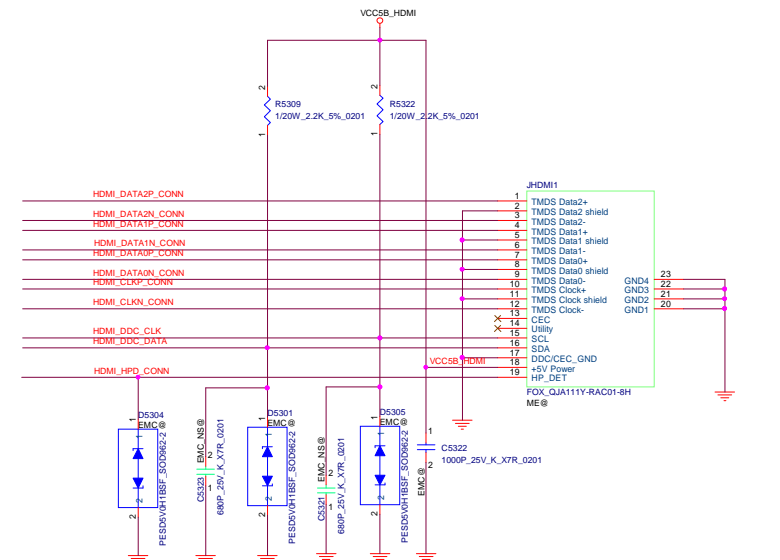
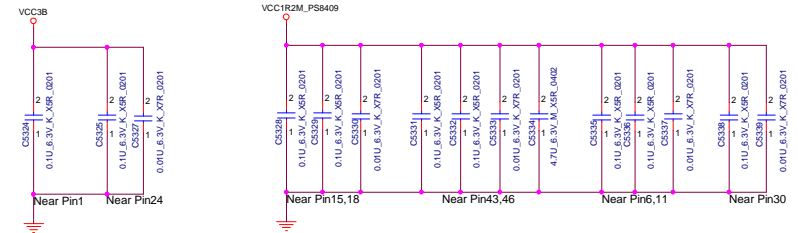
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|  | | |
| Project Name : T14s Gen2 | | Title : dGPU |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 49 of 130 |

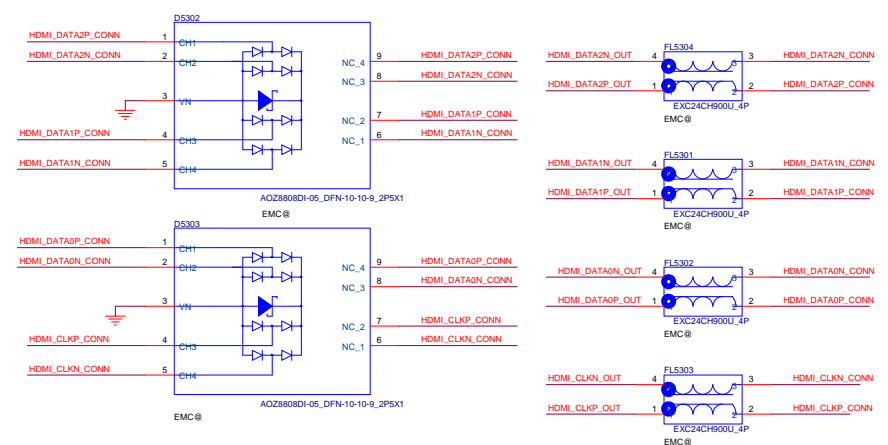


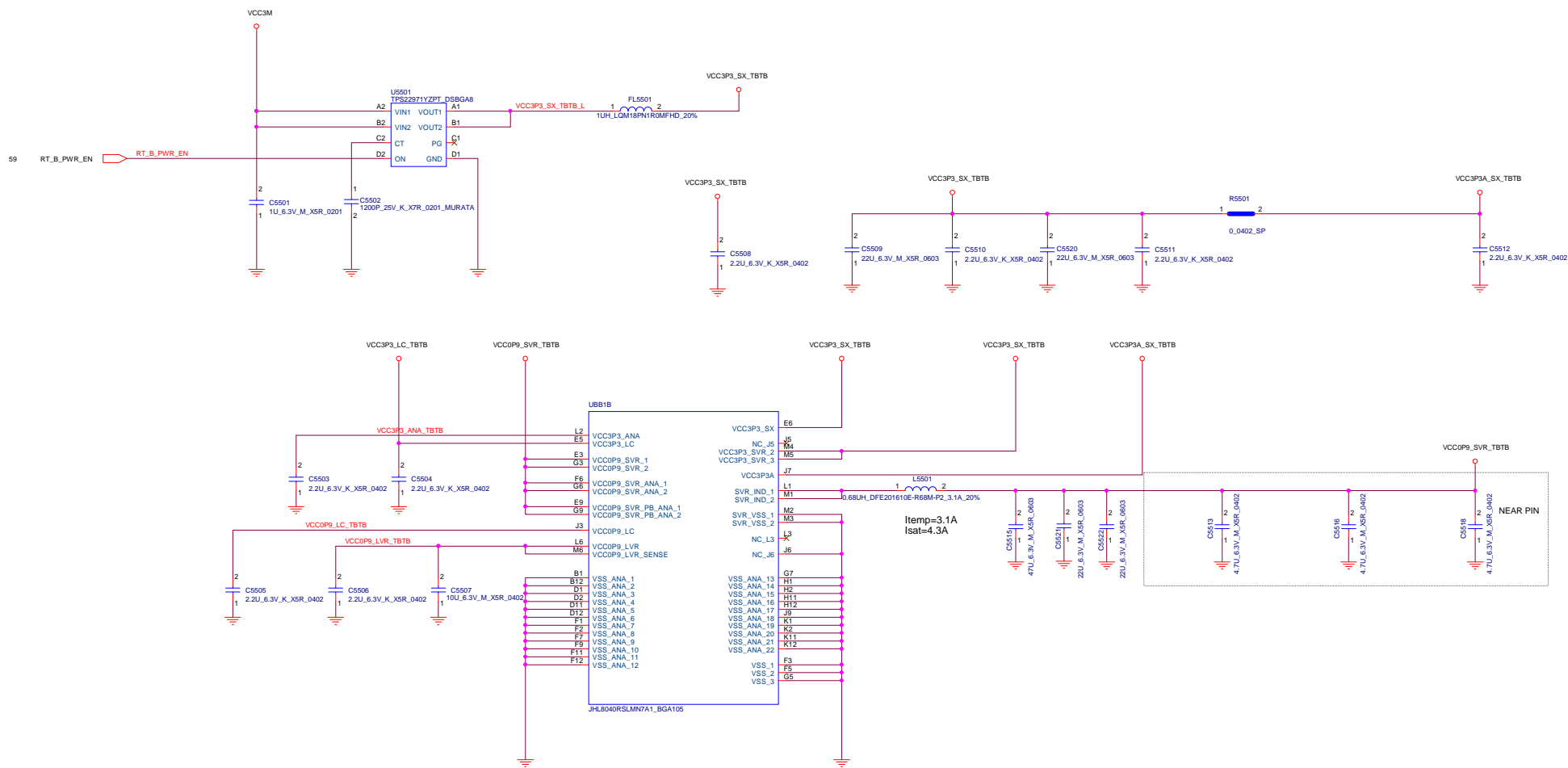
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|---------------------------------|-------------------|-------------------|
| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : dGPU |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 52 of 130 |



← Logic





Lenovo

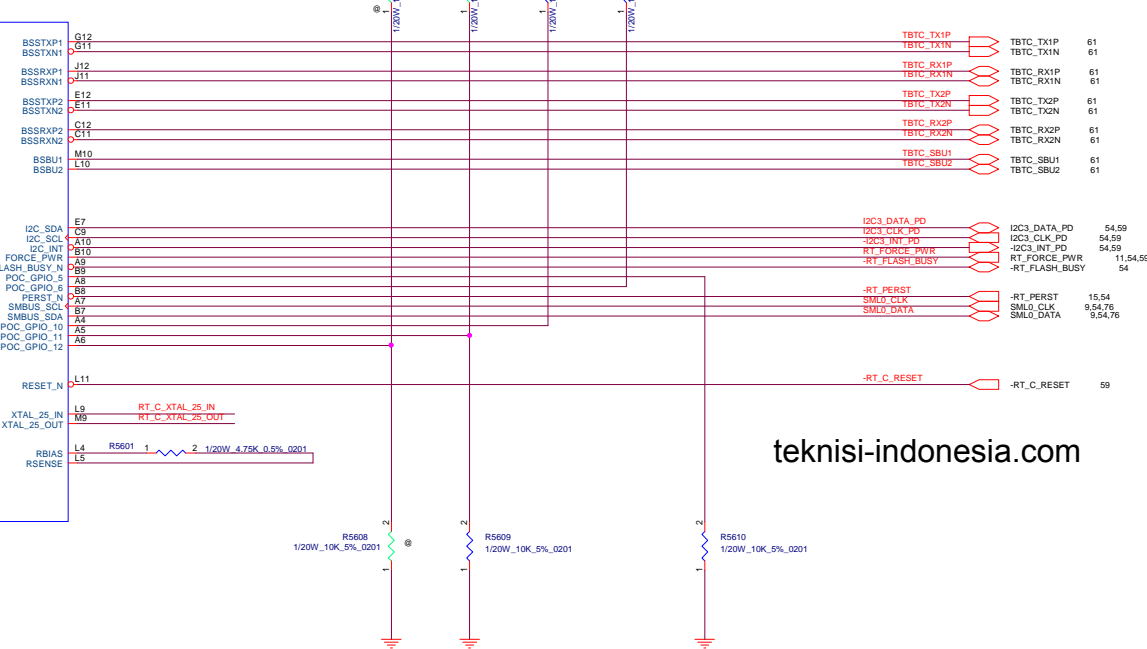
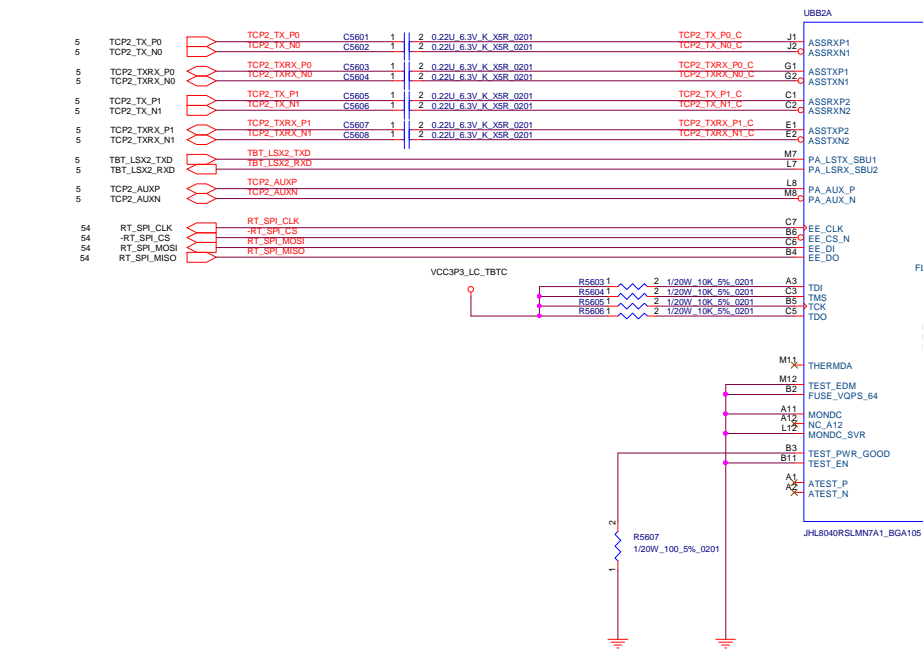


Table 8. Miscellaneous Signal and Pin Information

| Signal | Pin Number | Type | Power domain | Internal PU / PD | Fail-Safe | Description |
|--------------|------------|-------|--------------|------------------|-----------|--|
| I2C_SCL | C9 | I/O | POC | | Yes | I2C bus clock line |
| I2C_SDA | E7 | I/O | POC | | Yes | I2C bus data line |
| I2C_INT | A10 | OD | POC | | Yes | I2C bus interrupt |
| FORCE_PWR | B10 | I/O | POC | | Yes | GPIO Debug |
| FLASH_BUSY_N | A9 | I/O | POC | | Yes | GPIO Flash sharing control |
| POC_GPIO_5 | B9 | I/O | POC | | Yes | GPIO |
| POC_GPIO_6 | A8 | I/O | POC | | Yes | GPIO (should be connected to system S0 rail) |
| PERST_N | B8 | I/O | POC | | Yes | System PERST |
| SMBUS_SCL | A7 | I/O | POC | | Yes | SMBus clock |
| SMBUS_SDA | B7 | I/O | POC | | Yes | SMBus data |
| POC_GPIO_10 | A4 | I/O | POC | PU | Yes | GPIO (Used as Flash share strap) |
| POC_GPIO_11 | A5 | I/O | POC | PU | Yes | GPIO (Master-1/Slave-0 strap in Flash share mode) |
| POC_GPIO_12 | A6 | I/O | POC | PU | Yes | GPIO |
| RESET_N | L11 | I/O | POC | | | Main power reset signal |
| RBIAS | L4 | A-in | | | | External resistor for current biasing Resistor value 4.75KOhm +/- 0.5% |
| RSENSE | L5 | A-in | | | | Shares same external resistor as RBIAS |
| TEST_EDM | M12 | In | | | Yes | Testability signal, connect to GND |
| THERMDA | M11 | A-out | LC | | | Thermal Diode pin (anode) |
| NC_L3 | L3 | | | | | |

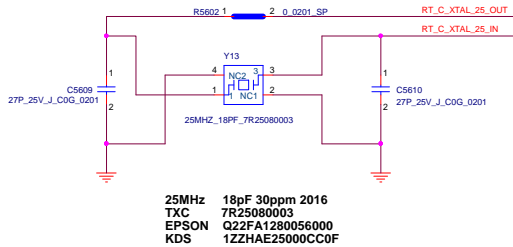


TABLE : Functional Strap

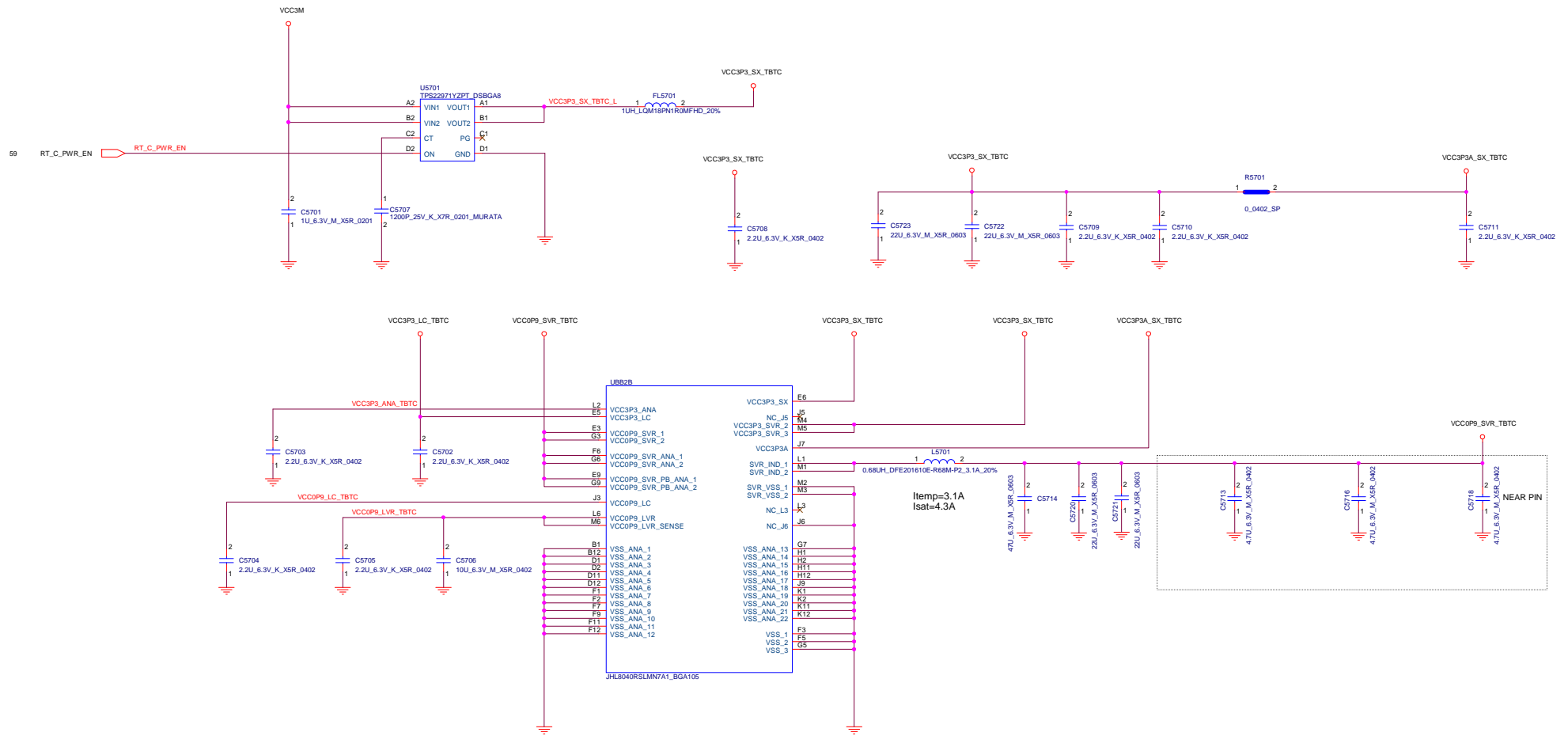
| POC_GPIO_10 (Flash Share Strap) | |
|---------------------------------|--|
| HIGH | Flash is shared between 2 Re-timers |
| LOW | Flash isn't shared. 1 Flash per Re-timer |

← LOGIC

TABLE : Functional Strap

| POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode) | |
|---|---|
| HIGH | Set Re-timer to be Master on shared flash SPI I/F |
| LOW | Set Re-timer to be Slave on shared flash SPI I/F |

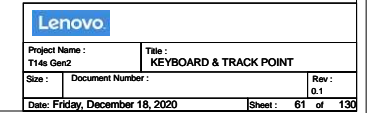
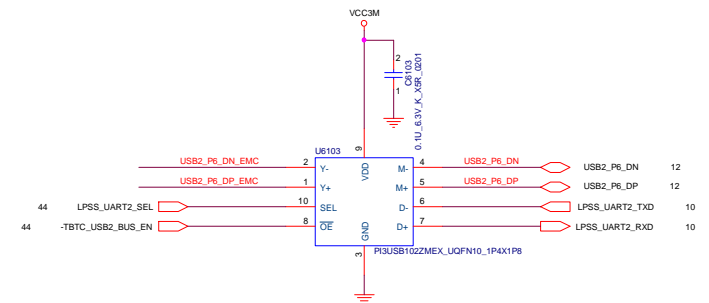
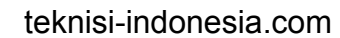
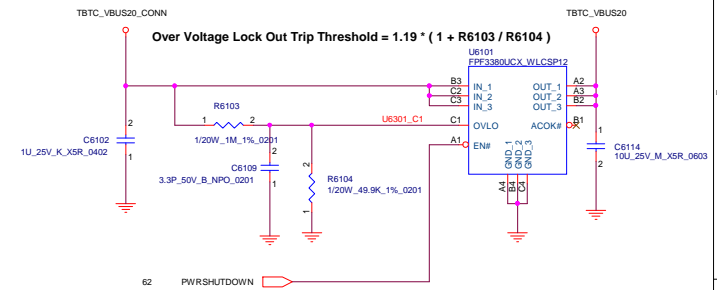
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| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : DDR VR |
| Size : C | Document Number : | Rev : 0.1 |
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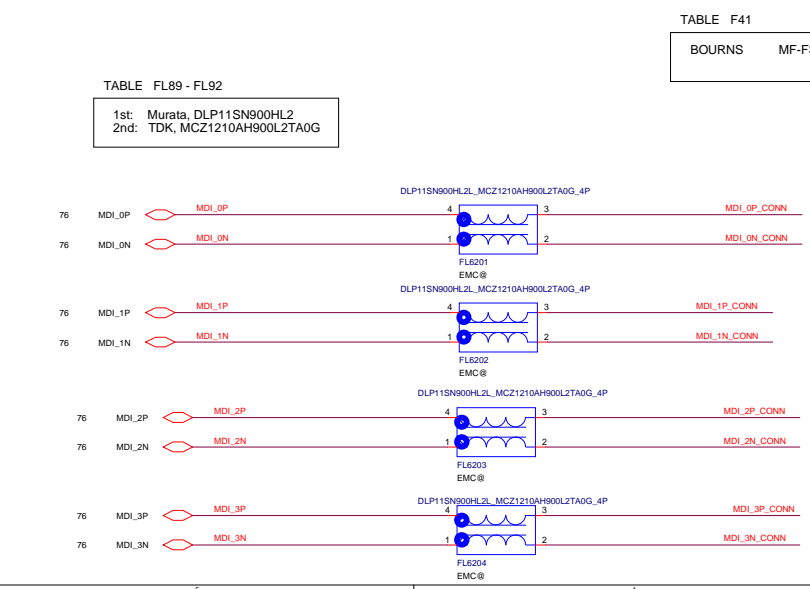
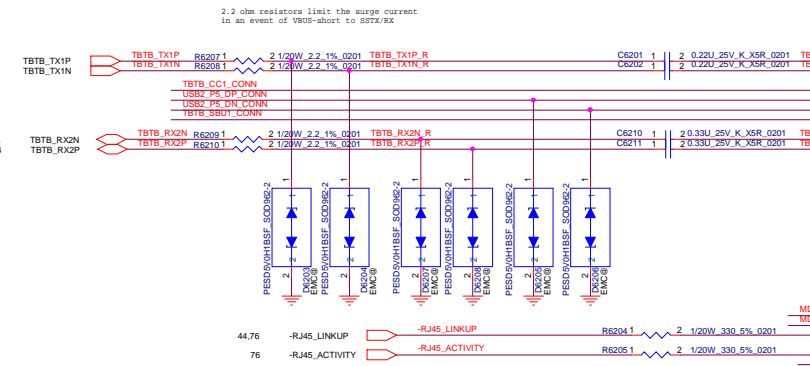
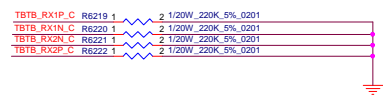
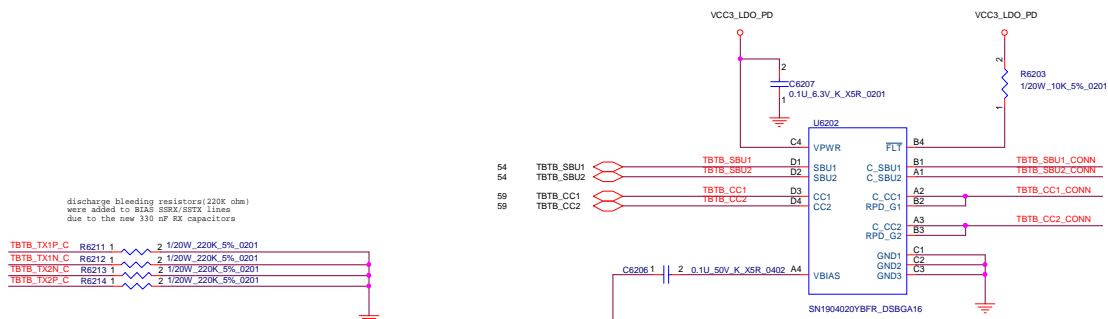


TABLE F41
BOURNS MF-FSMF035X-2

TABLE FL89 - FL92
1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G

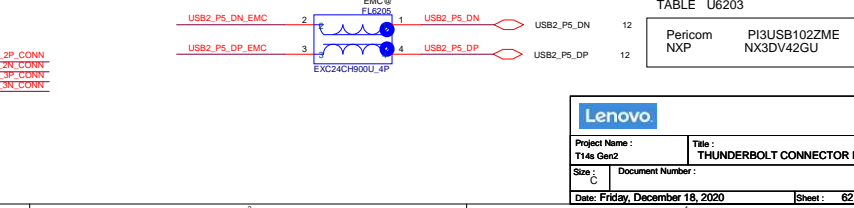
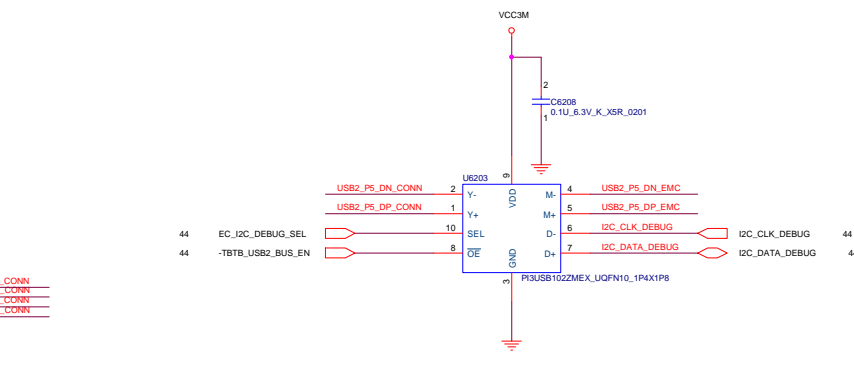
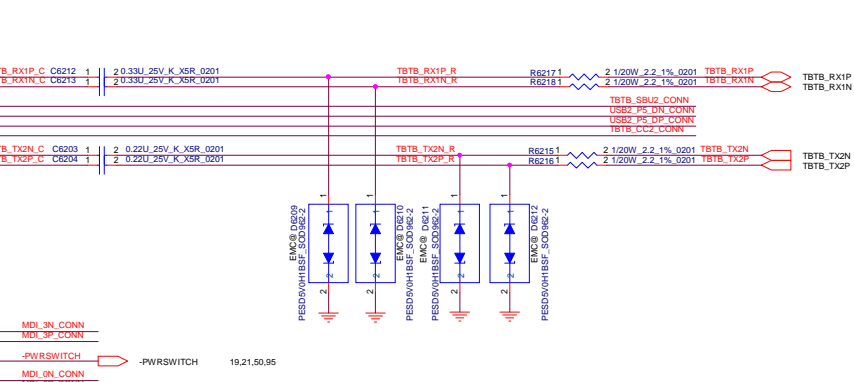
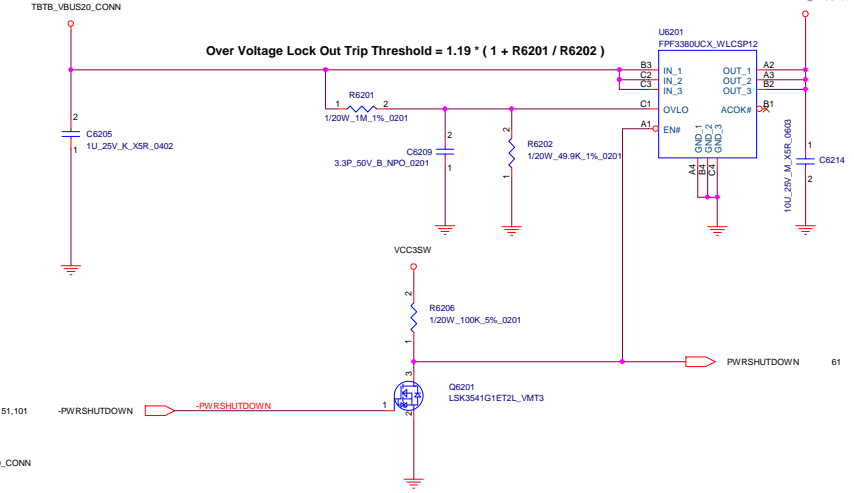
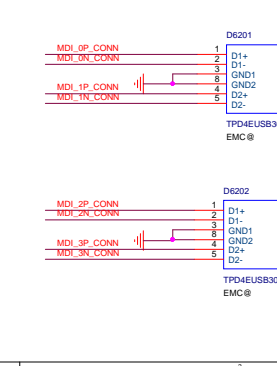
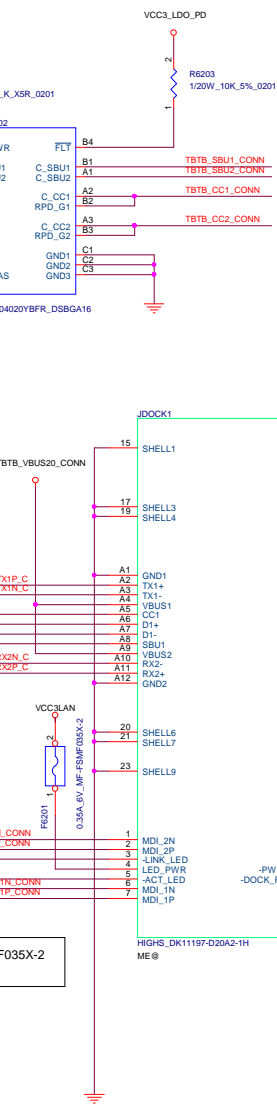


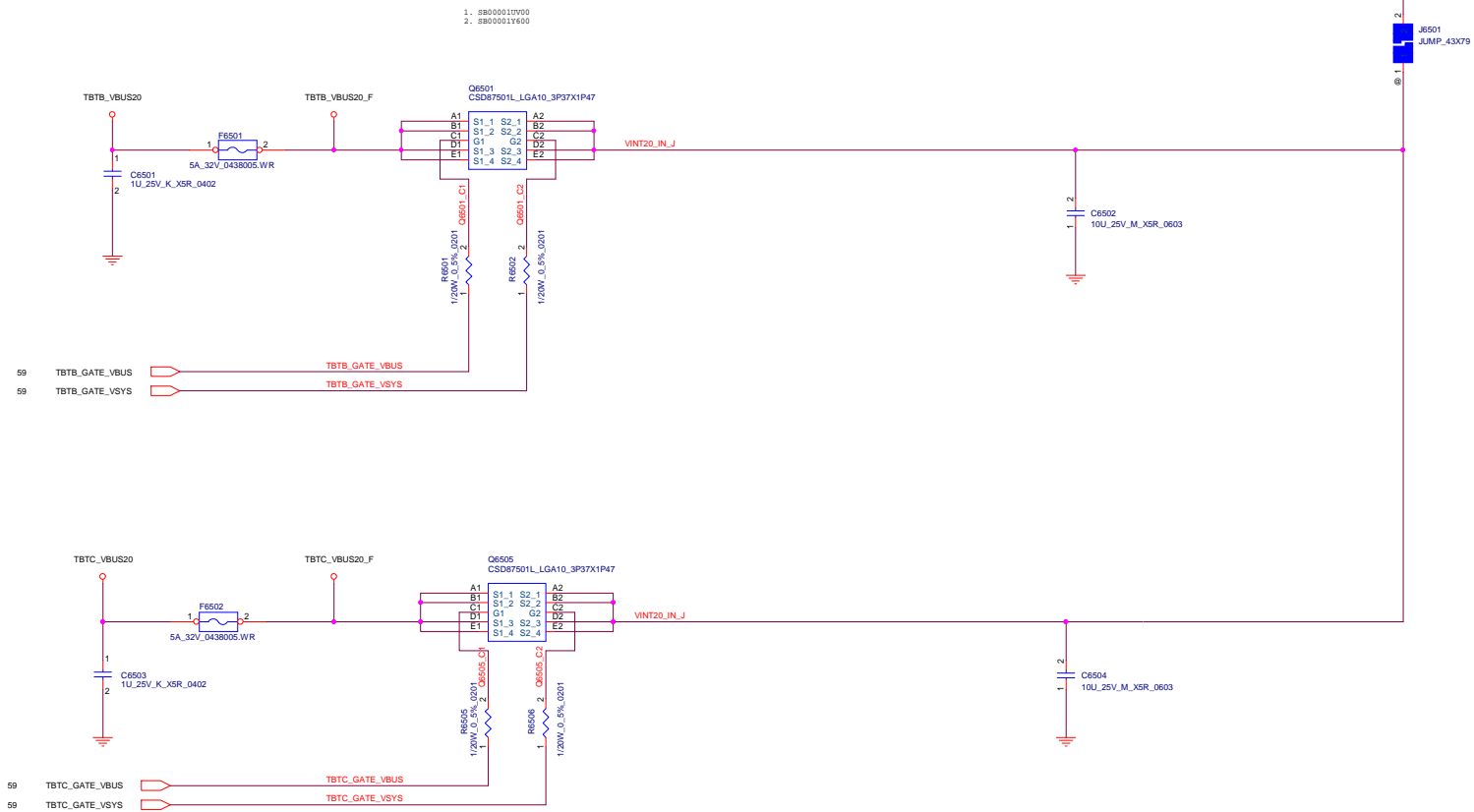
TABLE U6203
Pericom PI3USB102ZME NX3DV42GU

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| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : RJ45 Connector |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 63 of 130 |


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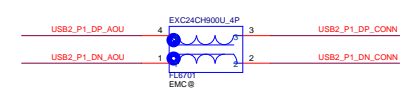
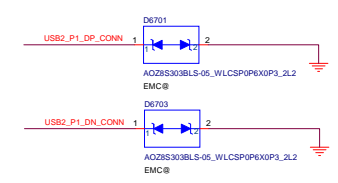
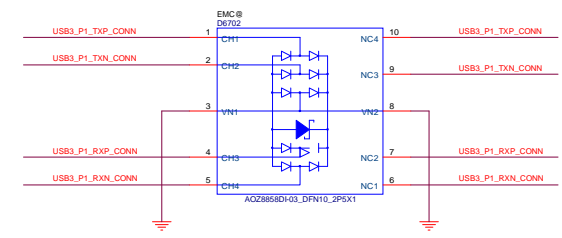
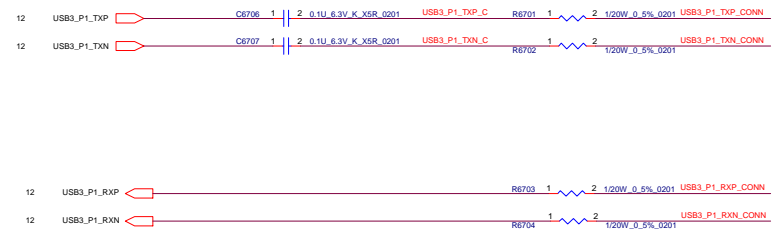
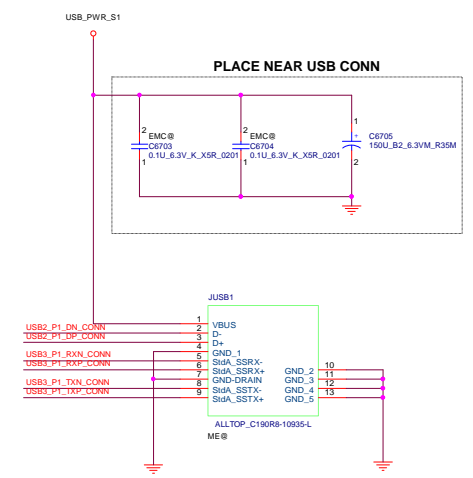
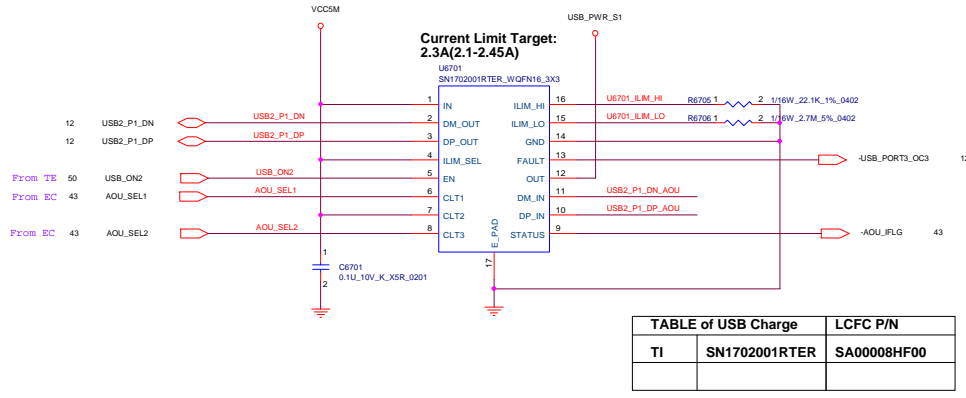
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| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : TOUCH PAD/NFC/FPR |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 64 of 130 |

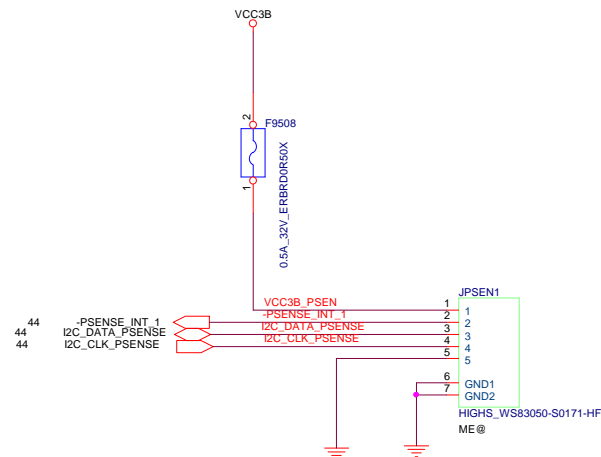
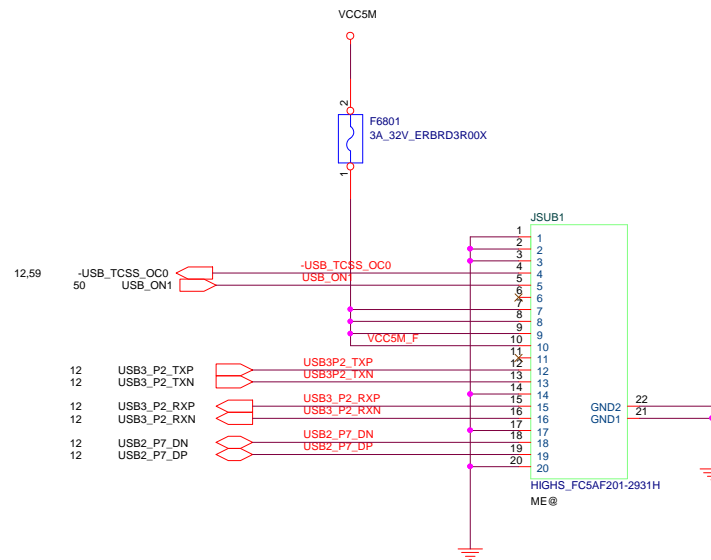


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| Project Name : T14s Gen2 | | Title : FAN CONNECTOR |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 66 of 130 |





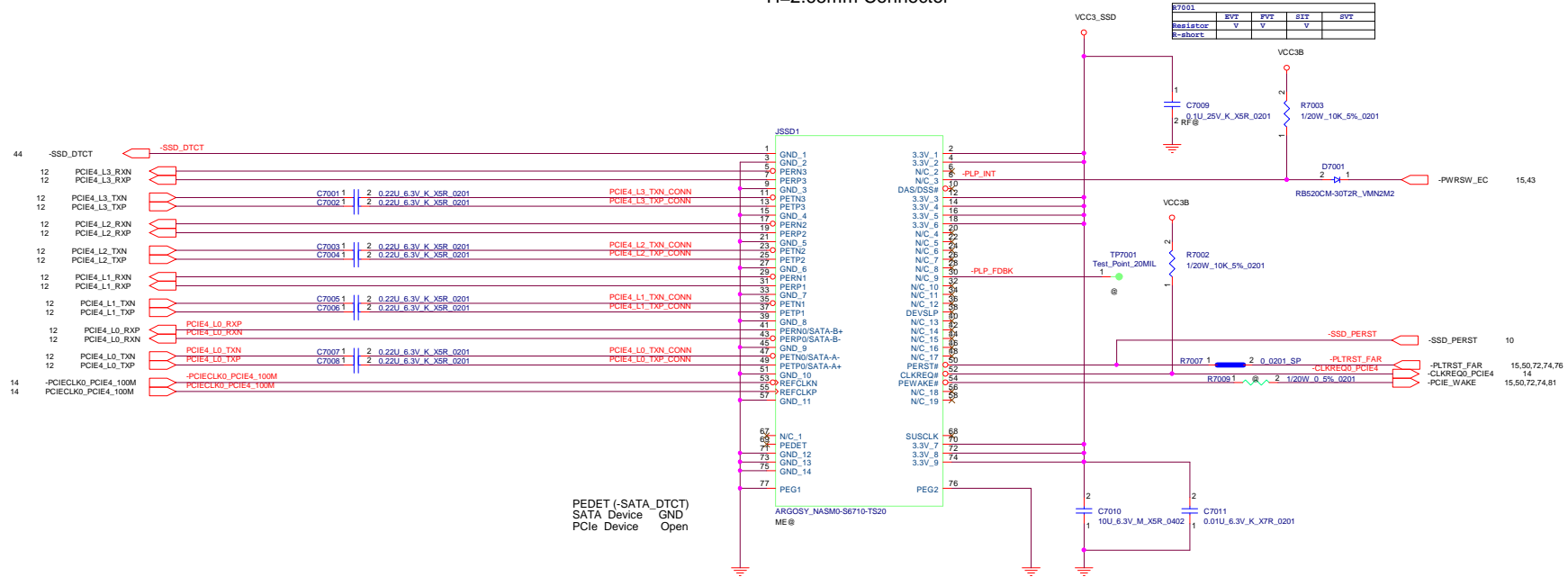
Pin assignment for P-sensor IC

| Pin Number | |
|------------|------------------------|
| 1 | VCC3B 3.3V (VDDHI) |
| 2 | PSENSE_INT (GPIO0/RDY) |
| 3 | I2C_CLK_PSENSE (SCL) |
| 4 | I2C_DATA_PSENSE (SDA) |
| 5 | GND (VSS) |


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| <div>Lenovo</div> | | |
| Project Name : T14s Gen2 | | Title : LAN Switch |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 69 of 130 |

M.2 Socket 3 (Key-M) for 2280 S3 SSD H=2.65mm Connector




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| Project Name : T14s Gen2 | | Title : SMBus Switch |
| Size : C | Document Number : | Rev : 0.1 |
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| Project Name : T14s Gen2 | | Title : dGPU |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 73 of 130 |

H=2.00mm Connector



EM160R-GL

Table 26: List of EM160R-GL Configuration Pins

EM120R-GL


Table 28: List of EM120R-GL Configuration Pins

EM05-CE


Table 18: List of Configuration Pins

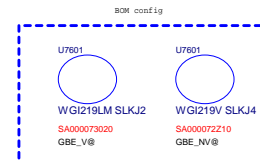
SDX55

1.5.1 Configuration Pins

| | | | | | | | |
|---|---------------------------|------------------------------|------------|-----------|-------------------------|------------|---|
| Security Classification | | LC Future Center Secret Data | | | Title | |  |
| Issued Date | 2018/01/12 | Deciphered Date | 2018/01/12 | | M.2 SOCKET 2 MODULE I/F | | |
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| Date: | Friday, December 14, 2020 | | [Sheet] | 74 of 130 | | | |

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| Project Name : T14s Gen2 | | Title : dGPU |
| Size : C | Document Number : | Rev : 0.1 |
| Date: Friday, December 18, 2020 | | Sheet : 75 of 130 |

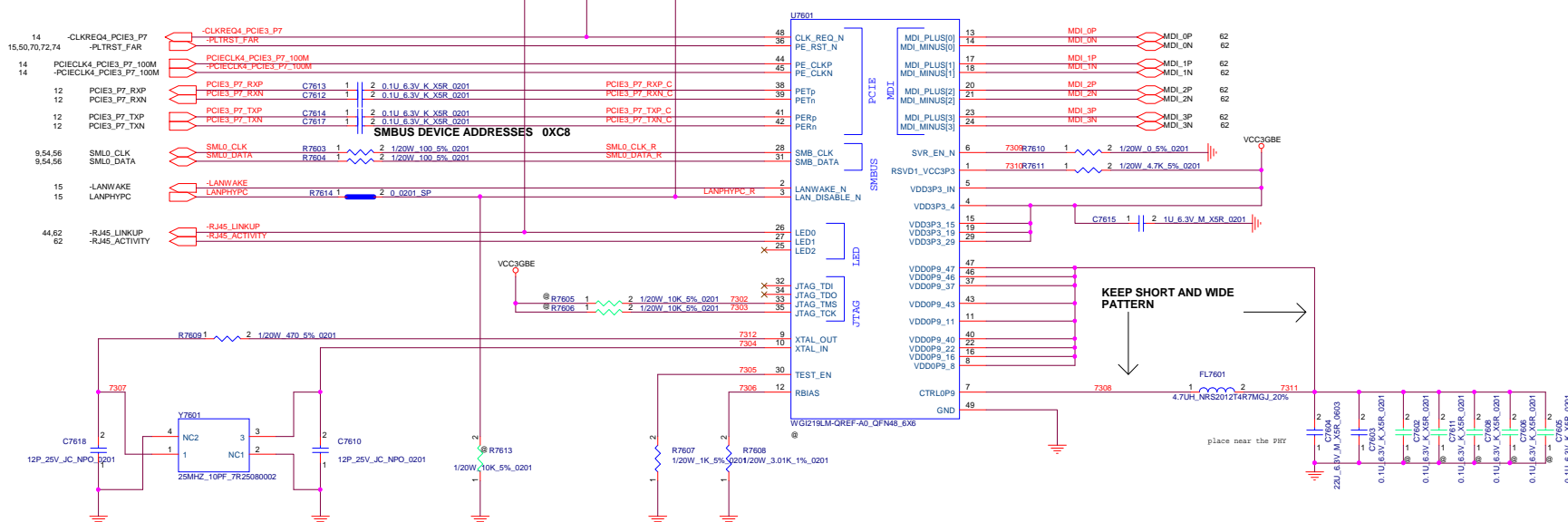


The I219's address is assigned using SMBus ARP protocol. The default SMBus address is 0xC8.


| SKU | Description | LCFC P/N |
|----------|----------------|-------------|
| vPRO | WGI219LM SLKJ2 | SA000073020 |
| non-vPRO | WGI219V SLKJ4 | SA000072Z10 |

| TABLE | | |
|---------|-----------------|----------------|
| 02D1 | vPro Capability | |
| GbE PHY | Yes | No |
| U7601 | Jacksonville-LM | Jacksonville-V |

LOGIC



| Y7601 CRYSTAL - 25MHz 10pF 30ppm 2016 | | |
|---------------------------------------|-----------------|-------------|
| Vendor | P/N | LCFC P/N |
| TXC | 7R25080002 | SJ10000PP00 |
| KDS | 1ZZHAE25000CC0B | SJ10000MN00 |
| Epson | Q22FA1280055900 | SJ10000PU00 |

| | | | | |
|---|------------------------------|-----------------|-------------------------------------|---|
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| | | | Date Friday, November 16, 2018 | Scale 76 in x 130 in |

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| Title | | |
| <Title> | | |
| Size | Document Number | Rev |
| Custom? (as Desc) | | 0.1 |
| Date: Friday, December 18, 2020 Sheet 77 of 130 | | |

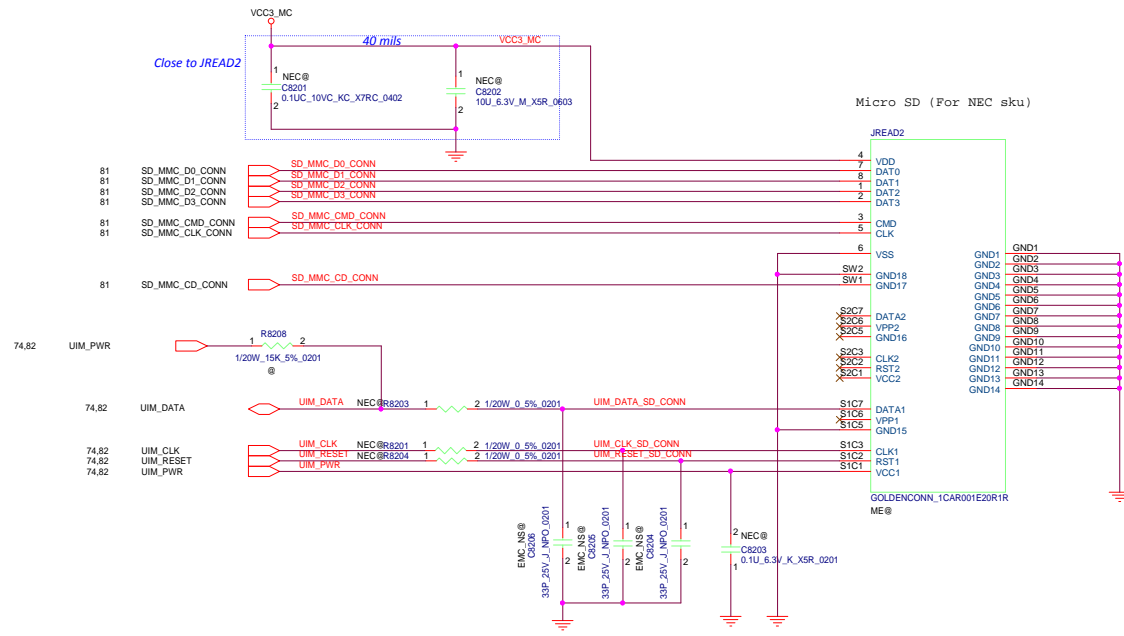
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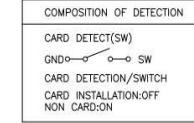
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| | | |
|-------------------|---------------------------|-----------------|
| Title | | |
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| Size | Document Number | Rev |
| Custom? (as Desc) | | 0.1 |
| Date: | Friday, December 18, 2020 | Sheet 80 of 130 |

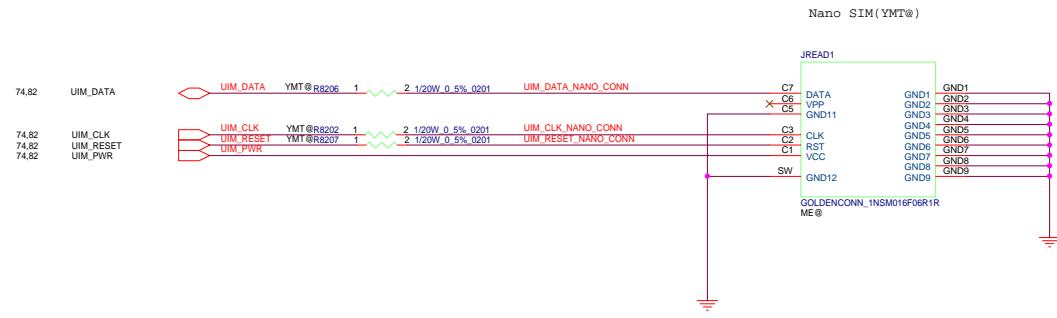


| Mode | Detect |
|-------------|--------|
| Normal | Short |
| Card Insert | Open |

1. ON SW接触GND 导通, SW断开GND OFF



2. 连接器插卡前SW是常闭状态



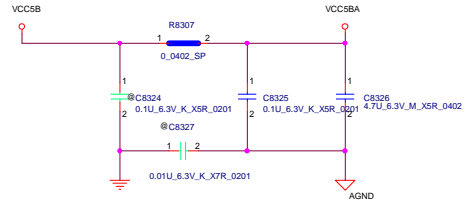
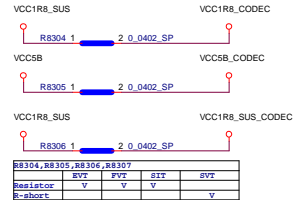
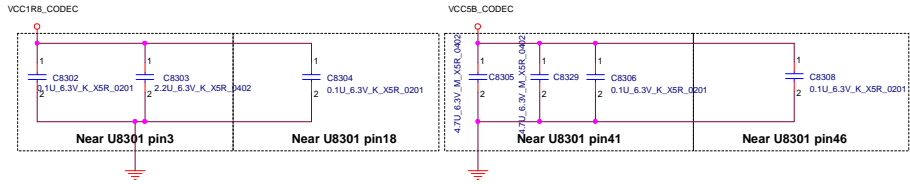
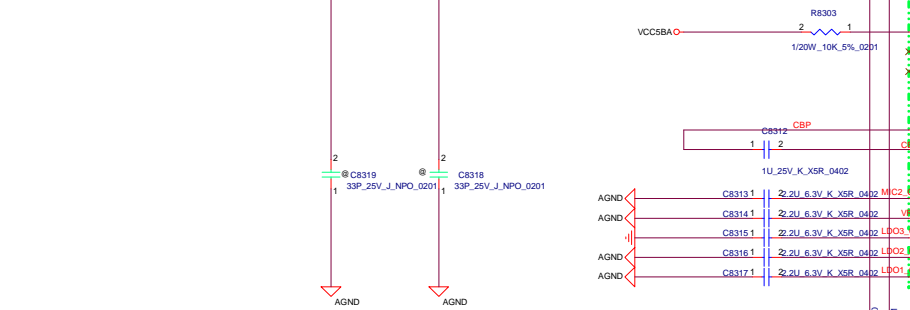
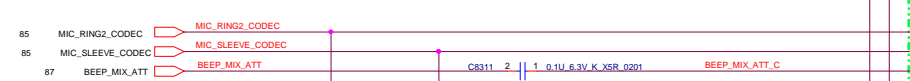
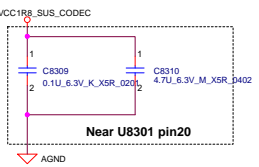
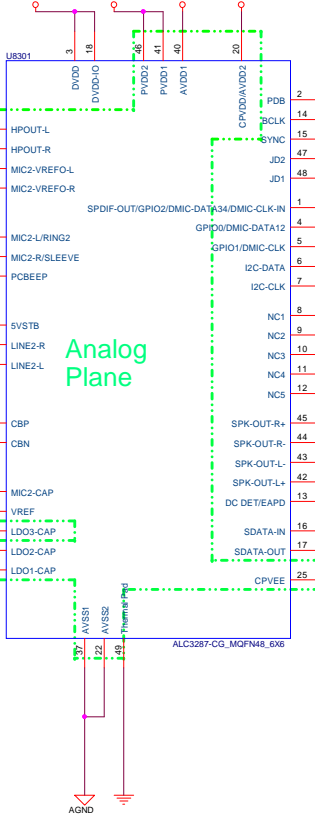


TABLE MIC HW ENABLE/DISABLE

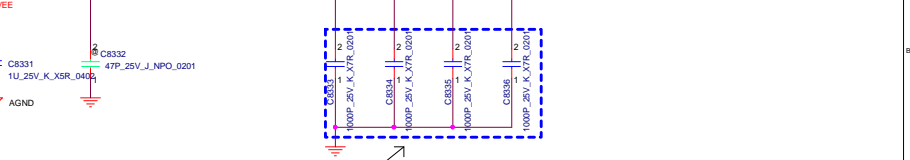
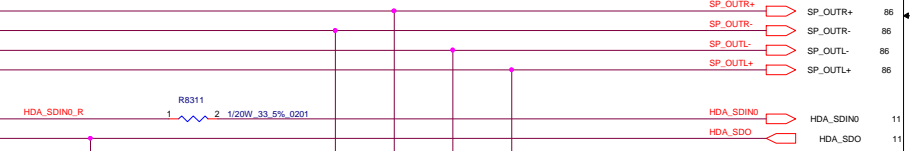
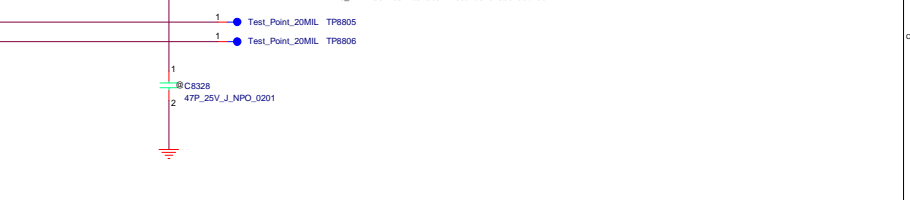
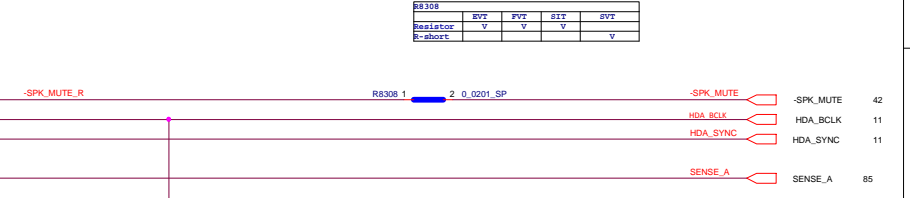
| | ENABLE | DISABLE |
|-------|--------|---------|
| R0805 | ASM | NO ASM |
| | ↑ | |
| | LOGIC | |



VCC1R8_CODEC VCC5B_CODEC VCC5BA VCC1R8_SUS_CODEC

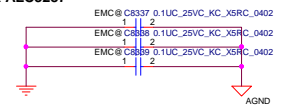


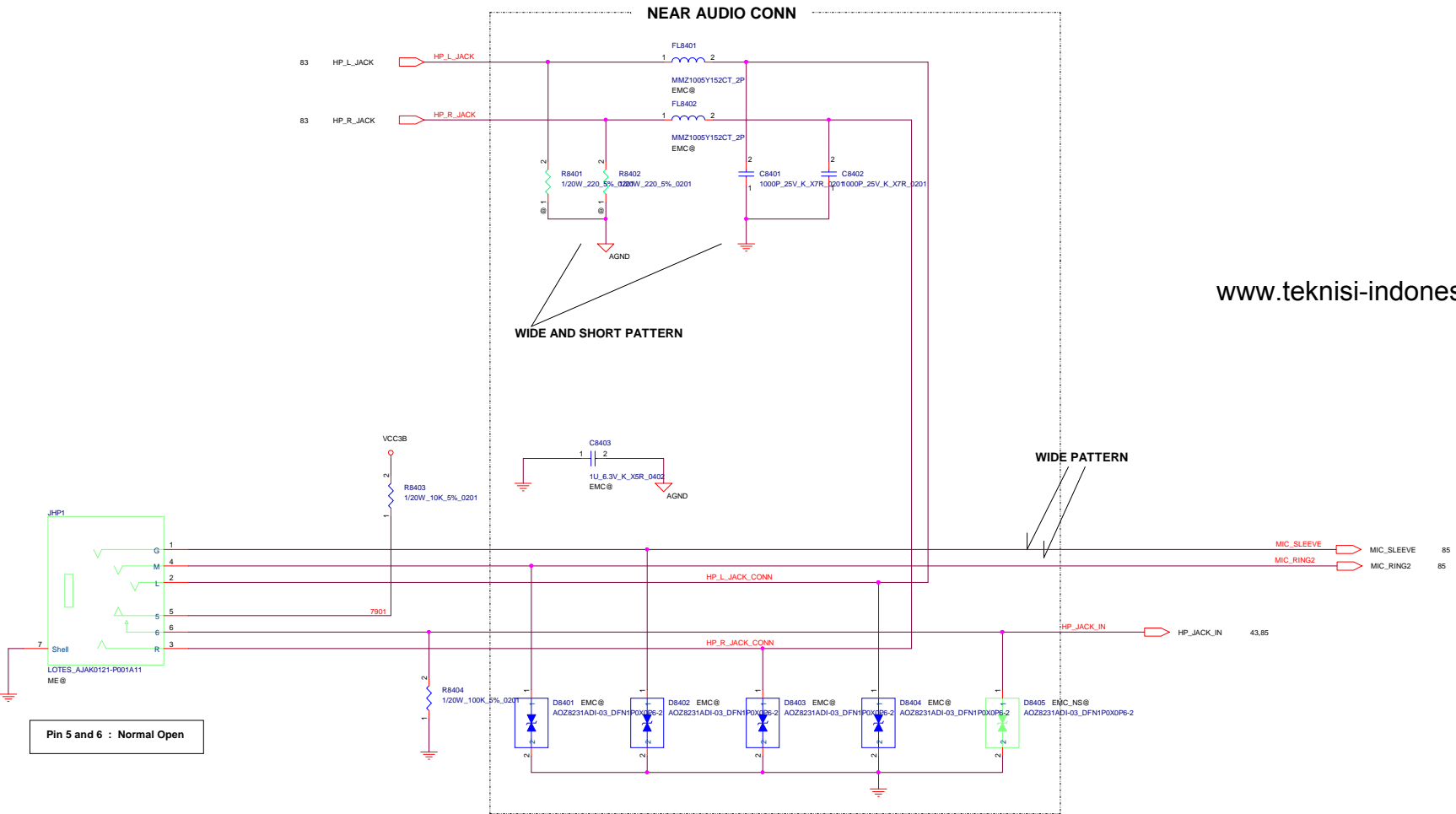
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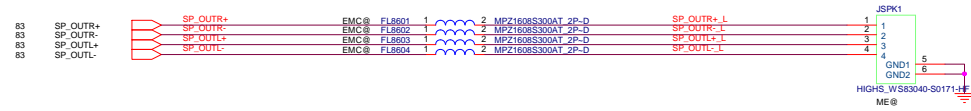
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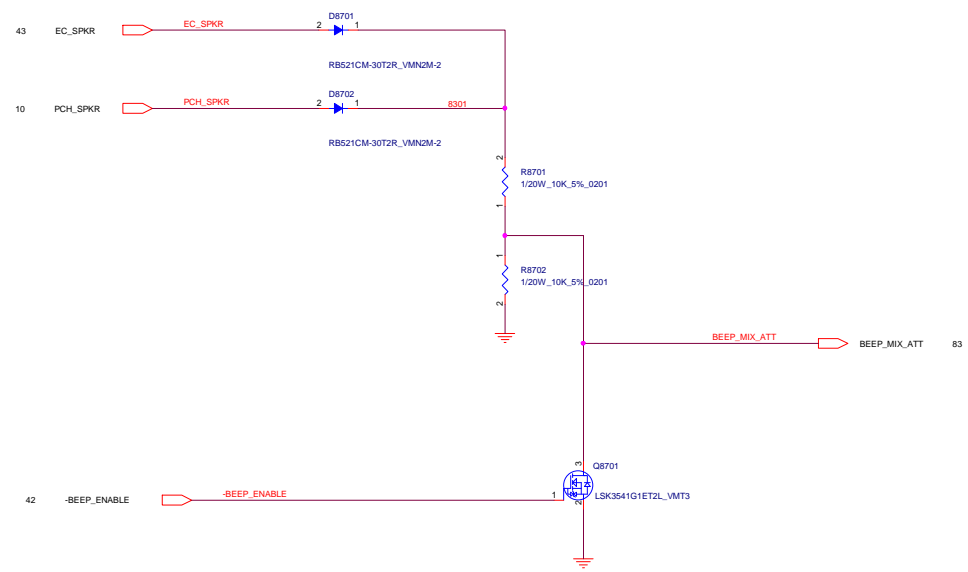
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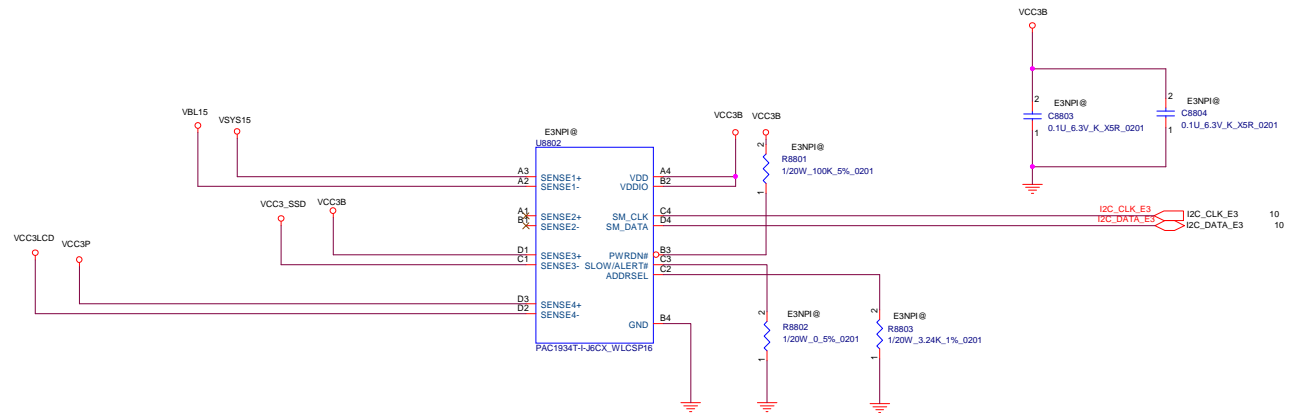




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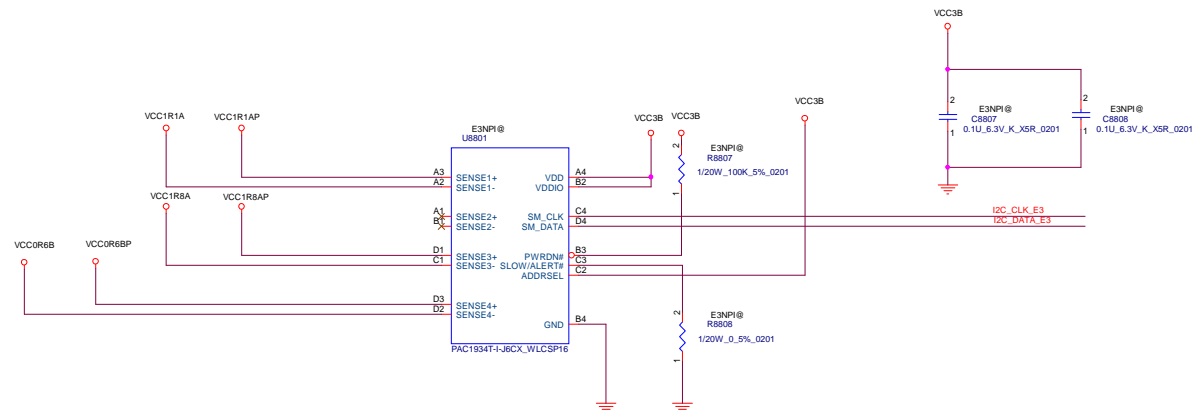






For LCD & Storage

I2C Address:0010_101(ADDRSEL=3,240)



For DDR

I2C Address:0011_111(ADDRSEL=Tied to VDD)

I2C Address:0011_010(ADDRSEL=34,000)

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| Size | Document Number | Rev |
| Customer | 146 Gen2 | 0.1 |
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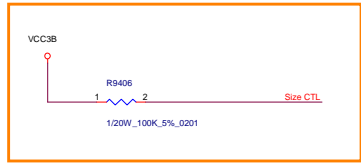
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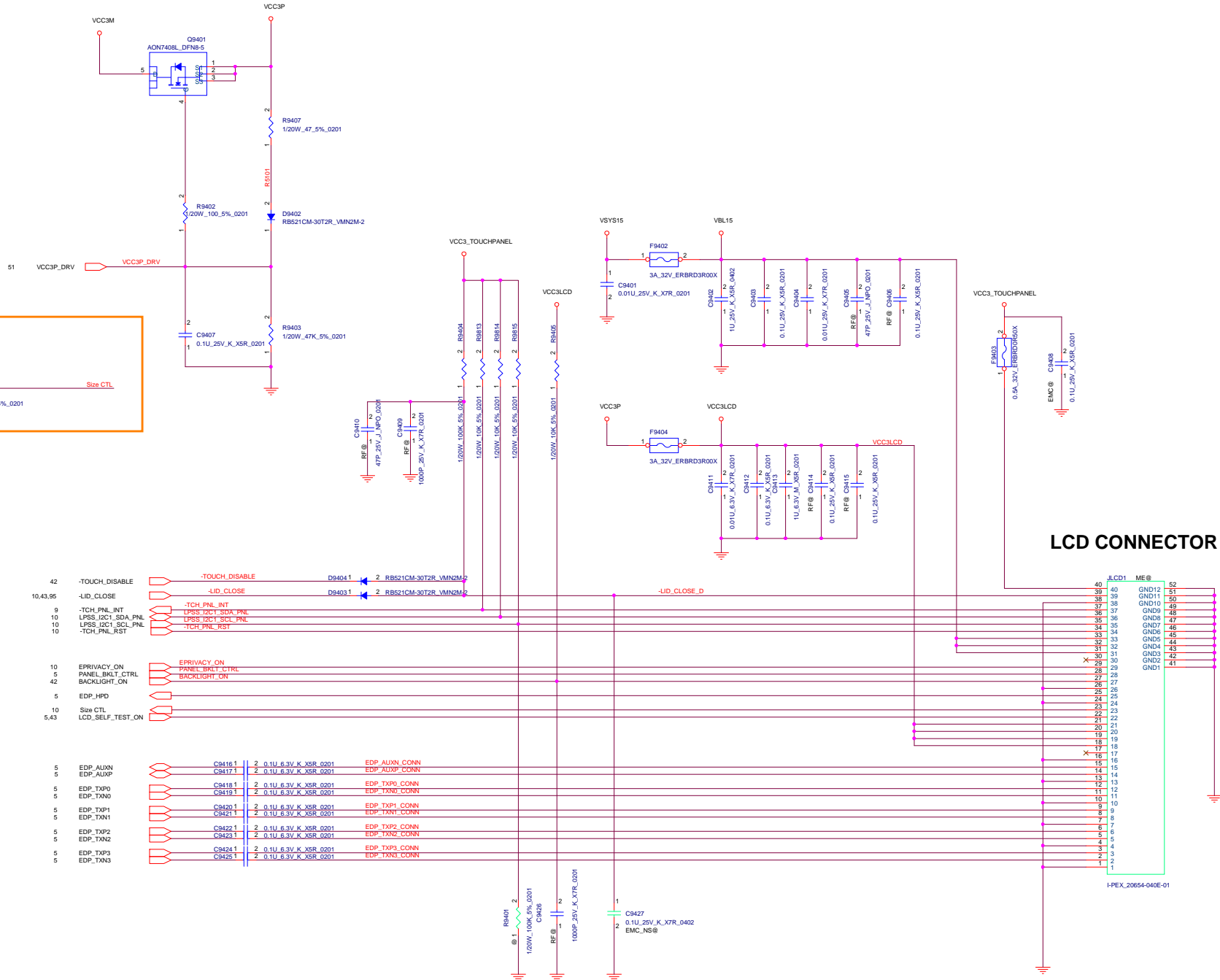
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| Issued Date | | 2018/01/12 | Deciphered Date | 2018/01/12 | SCR&FPR&NEC LED | |
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| Date: Friday, December 18, 2020 | | | | | Sheet 93 of 130 | |

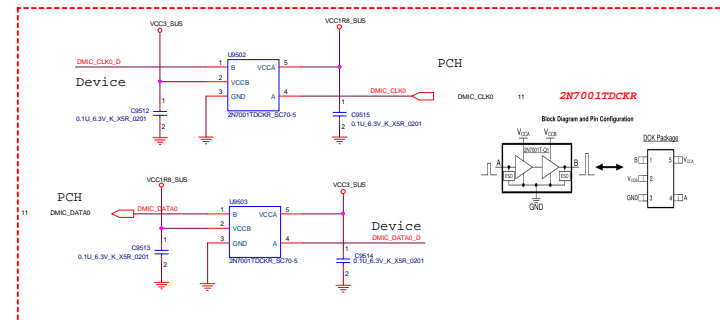
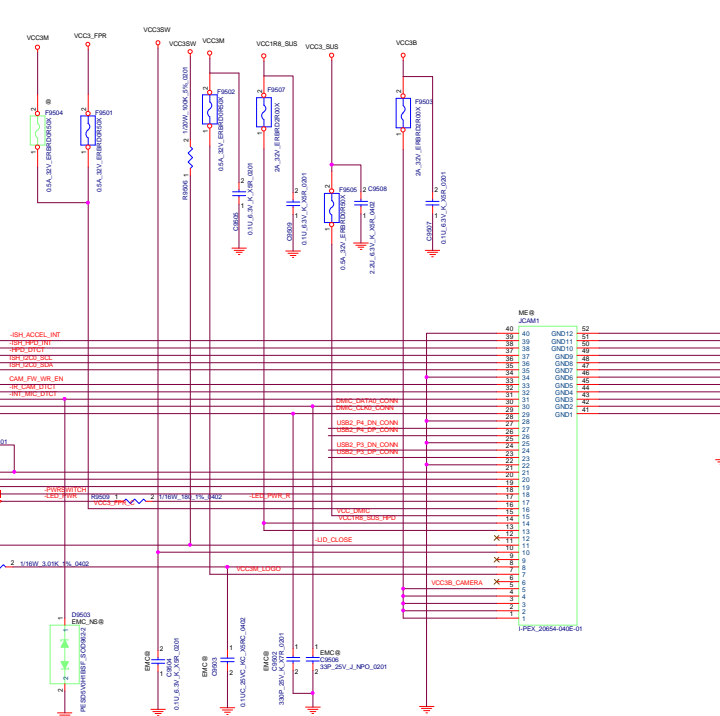
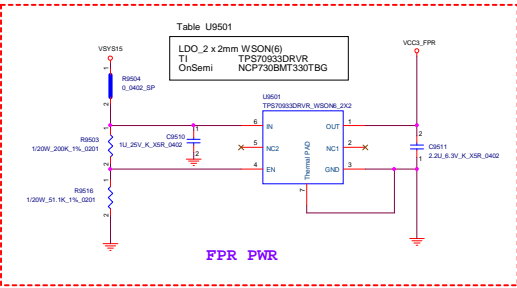


LCD size control
Low:14" TIGER
High:13" SERVAL

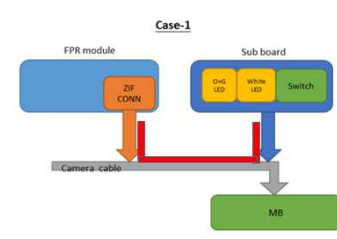
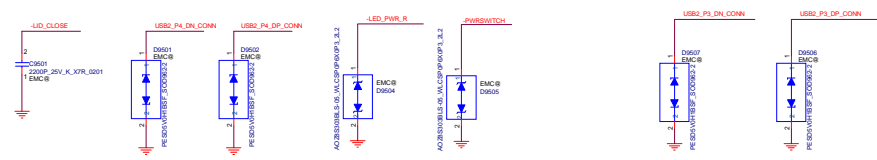


LCD CONNECTOR

| | | | | | | | | | | |
|---|------------|------------------------------|------------|--|---------------|-----------------|---|---------------------------|--|--|
| Security Classification | | LC Future Center Secret Data | | | Title | |  | | | |
| Issued Date | 2018/01/12 | Deciphered Date | 2018/01/12 | | LCD INTERFACE | | | | | |
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| | | | | | Date | | | Friday, December 18, 2020 | | |
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WTB - Camera
 - FPR
 - PWR SUB BD
 -Hall Sensor



For HPD

| PIN | SIGNAL NAME |
|-----|---------------|
| 1 | SIG 5PIN |
| 2 | ISH I2C0_SCL |
| 3 | ISH I2C0_SDA |
| 4 | VCC1R8_SUS_HP |
| 5 | -ISH HPD_INT |

For Hybrid & RGB

| No. | Pin assignment | No. | Pin assignment |
|-----|----------------|-----|----------------|
| 17 | IR VCC | 18 | IR VCC |
| 1 | MIC DET | 16 | MIC VCC |
| 2 | *WP | 15 | MIC CLK |
| 3 | NC | 14 | MIC DATA |
| 4 | NC | 13 | NC |
| 5 | CAM 3V3 | 12 | CAM 3V3 |
| 6 | *Reverse | 11 | D+ |
| 7 | MIC GND | 10 | D- |
| 8 | DOND | 9 | DOND |
| 19 | IR GND | 20 | IR GND |

For FPR

| GPIO | State | GPIO | Input/Output | S0 | S3 | S4 | S5 |
|-------------|-------|----------------------|--------------|------|-----|-----|-----|
| GPIO_AL0 | High | Disable Power Button | Output | Low | Low | Low | Low |
| GPIO_AL0 | Low | Enable Power Button | Output | Low | Low | Low | Low |
| DELINK | High | S0/S3/S4/S5 | Input | High | Low | Low | Low |
| FPS_RESET_N | Low | Reset | Input | High | Low | Low | Low |

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| Date: | Friday, December 18, 2020 | Sheet 96 of 130 | |

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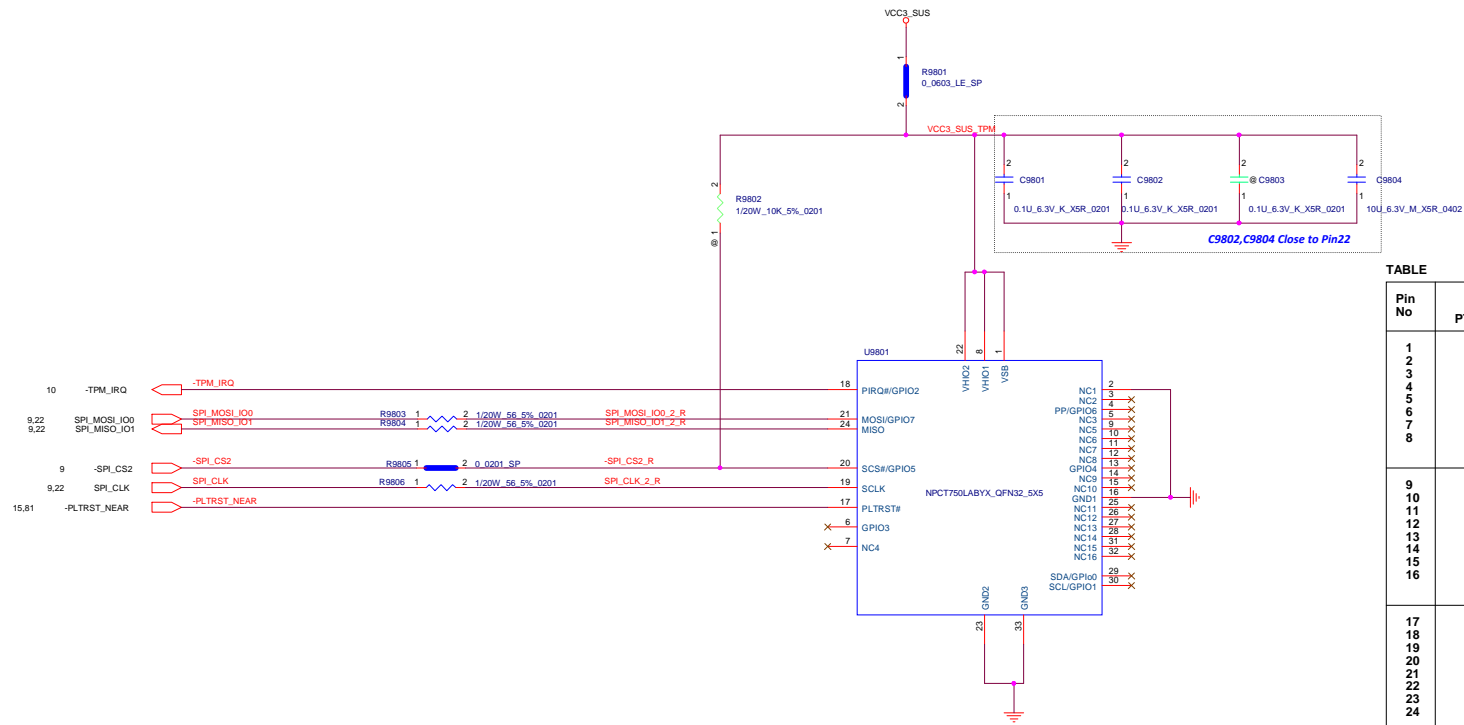
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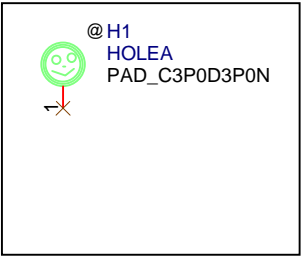
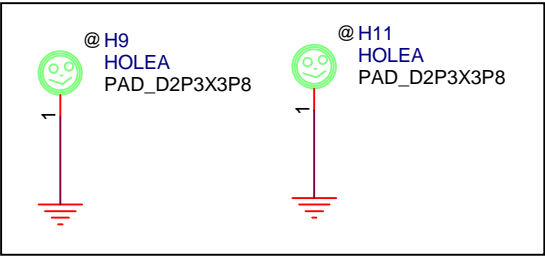
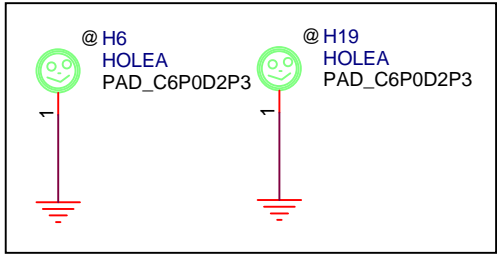
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|----------------------|------------------|-------------|
| Vendor | P/N | LCFC P/N |
| ST Micro | ST33HTPH2X32AHD4 | SA0000AB710 |
| Nuvoton | NPCT750LABYX QFN | SA00008KS20 |
| ST Micro | ST33HTPH2X32AHD8 | SA0000AB720 |
| Nuvoton | NPCT750LADYX QFN | SA00008KS30 |

Pre FVT

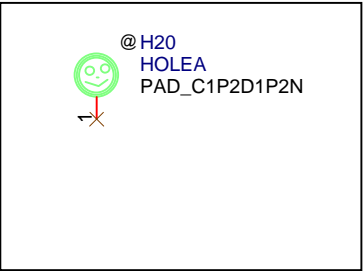
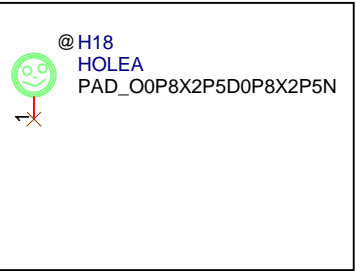
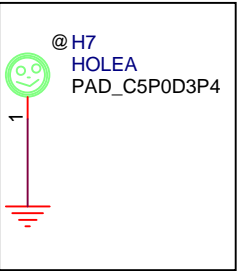
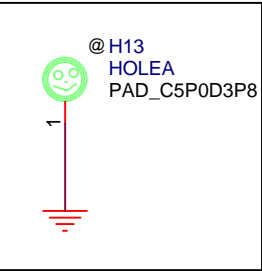
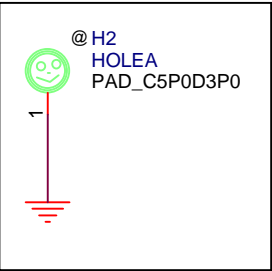
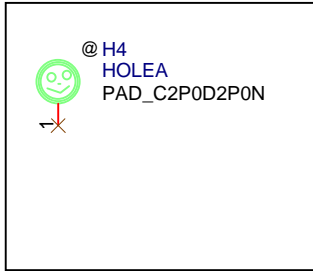
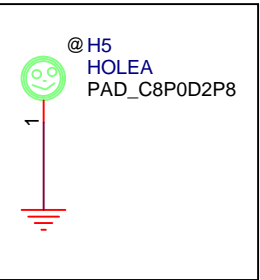
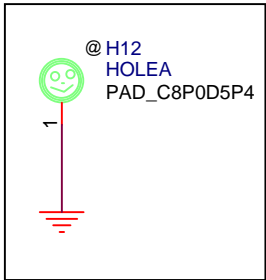
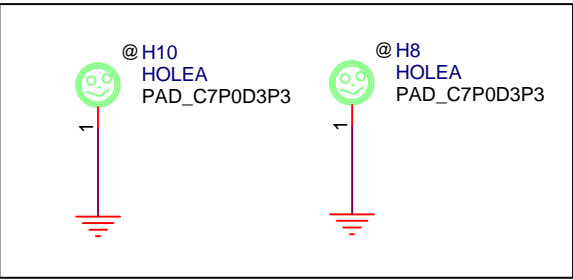
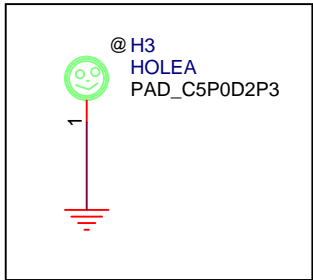
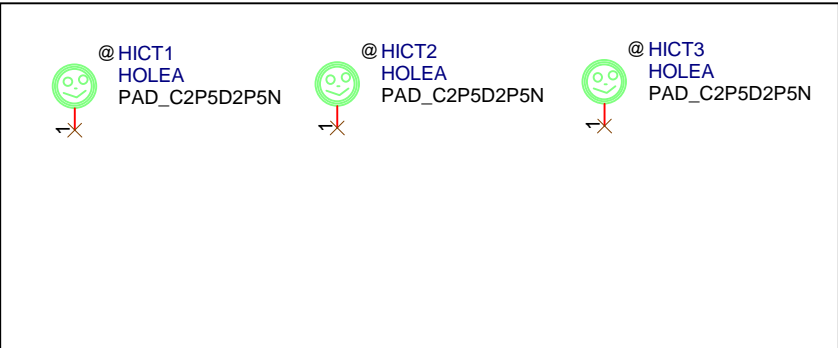
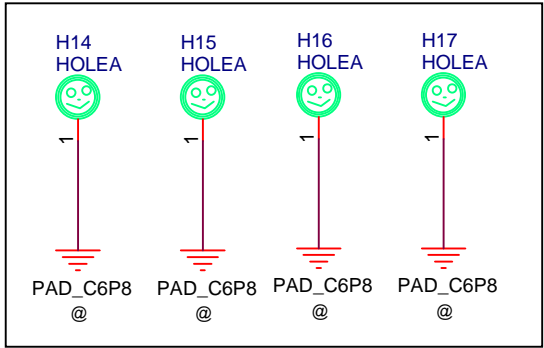
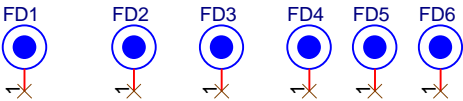
FVT and after

TABLE

| Pin No | TCG PTP Spec (v38) | Nuvoton NPCT750LABYX | ST Micro ST33HTPH2X32AHD4 |
|--------|--------------------|----------------------|---------------------------|
| 1 | VDD | VS8 | NC |
| 2 | GND | NC | GND |
| 3 | NC | NC | NC |
| 4 | GPIO | GPIO/PP | PP |
| 5 | NC | NC | NC |
| 6 | GPIO | GPIO3 | NC |
| 7 | GPIO | NC | GPIO |
| 8 | VDD | VHIO | NC |
| 9 | NC | NC | NC |
| 10 | NC | NC | NC |
| 11 | NC | NC | NC |
| 12 | NC | NC | NC |
| 13 | GPIO | GPIO4 | NC |
| 14 | NC | NC | NC |
| 15 | NC | NC | NC |
| 16 | GND | GND | NC |
| 17 | SPI_RST# | RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ#/GPIO2 | SPI_PIRQ# |
| 19 | SPI_CLK | SCLK | SPI_CLK |
| 20 | SPI_CS# | SCS#/GPIO5 | SPI_CS# |
| 21 | MOSI | MOSI/GPIO7 | MOSI |
| 22 | VDD | VHIO | VPS |
| 23 | GND | GND | NC |
| 24 | MISO | MISO | MISO |
| 25 | NC | NC | NC |
| 26 | NC | NC | NC |
| 27 | NC | NC | NC |
| 28 | NC | NC | NC |
| 29 | SDA/GPIO1 | SDA/GPIO1 | NC |
| 30 | SDA/GPIO0 | SDA/GPIO0 | NC |
| 31 | NC | NC | NC |
| 32 | NC | NC | NC |

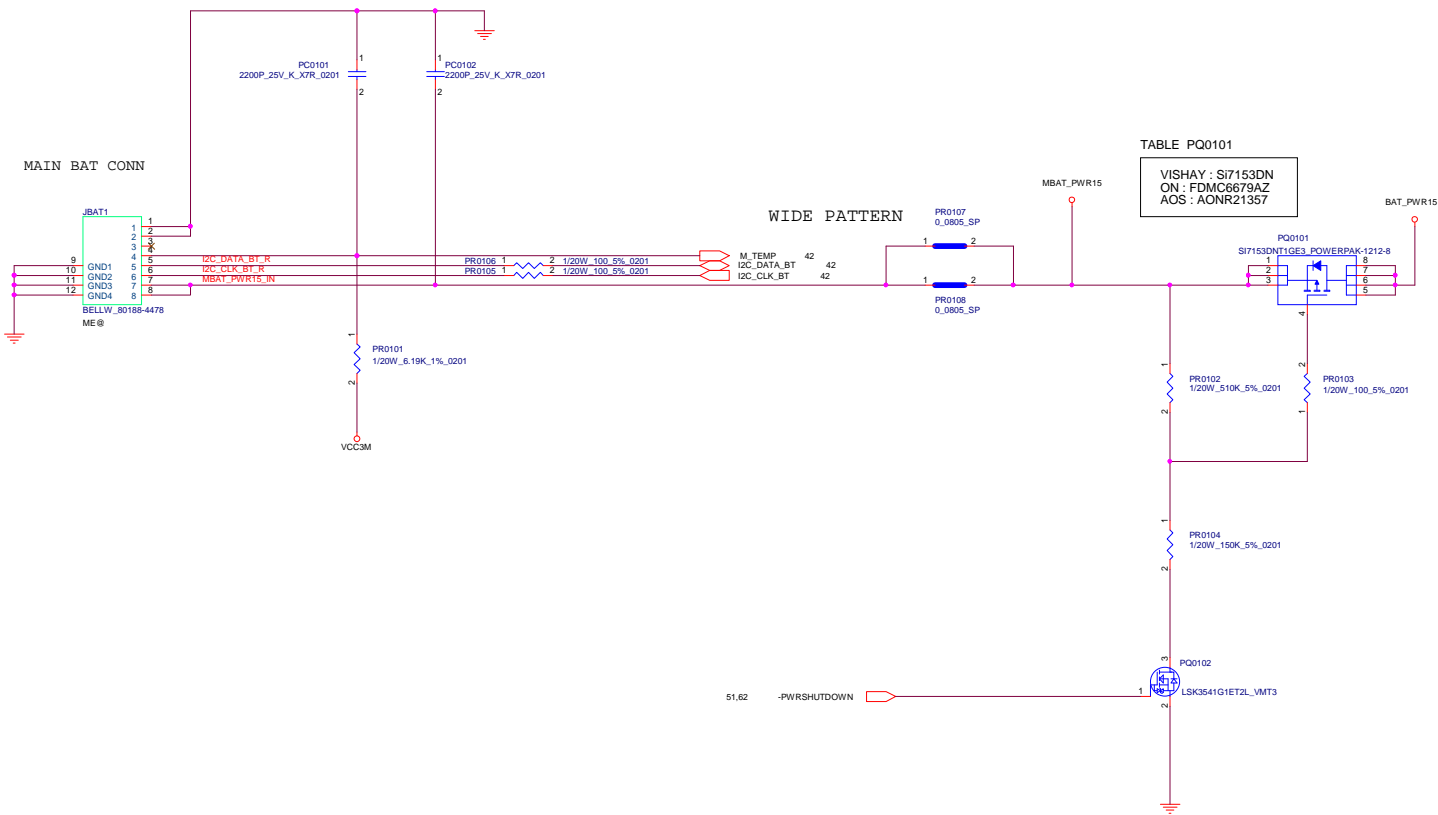


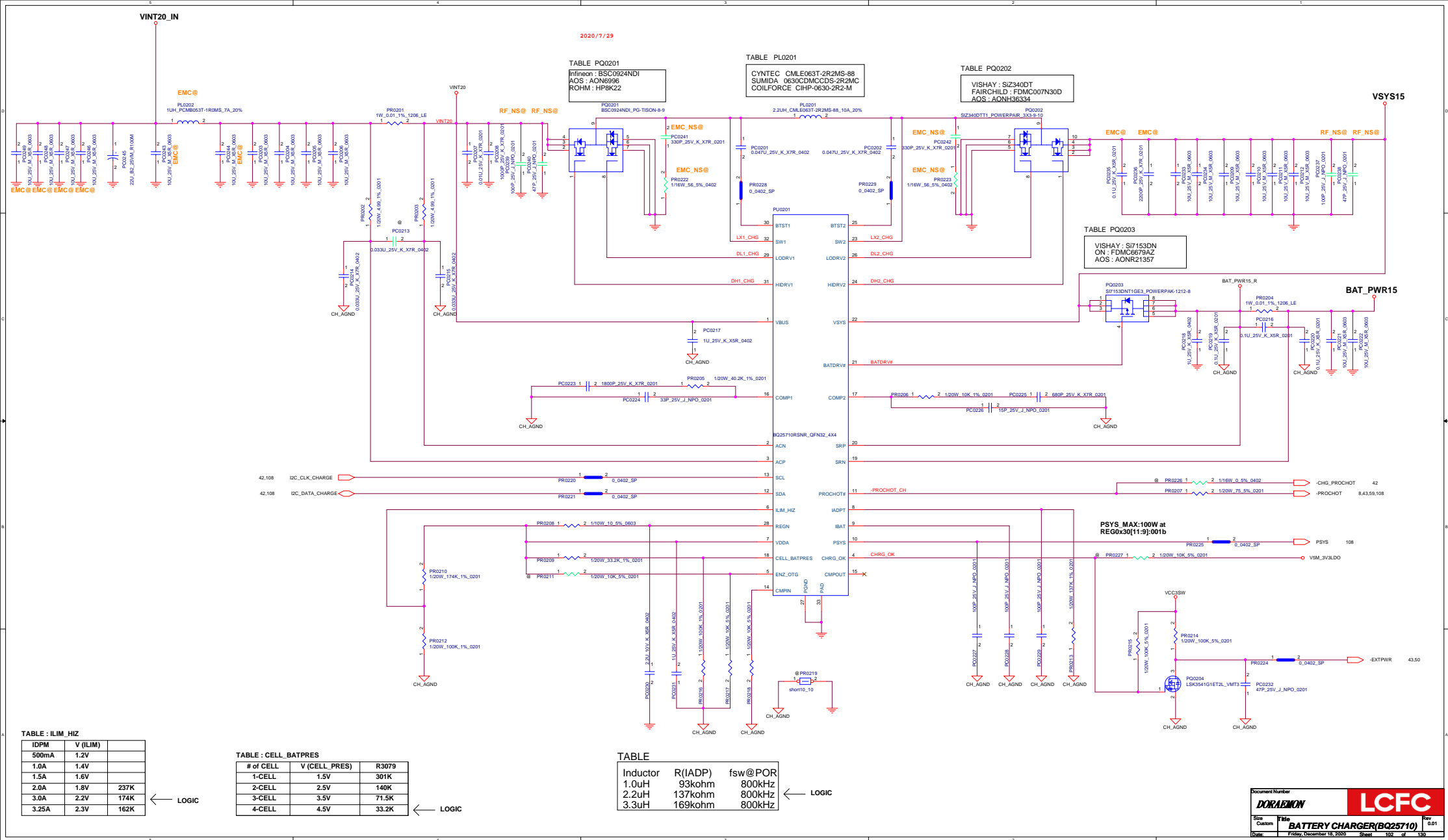
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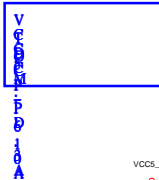
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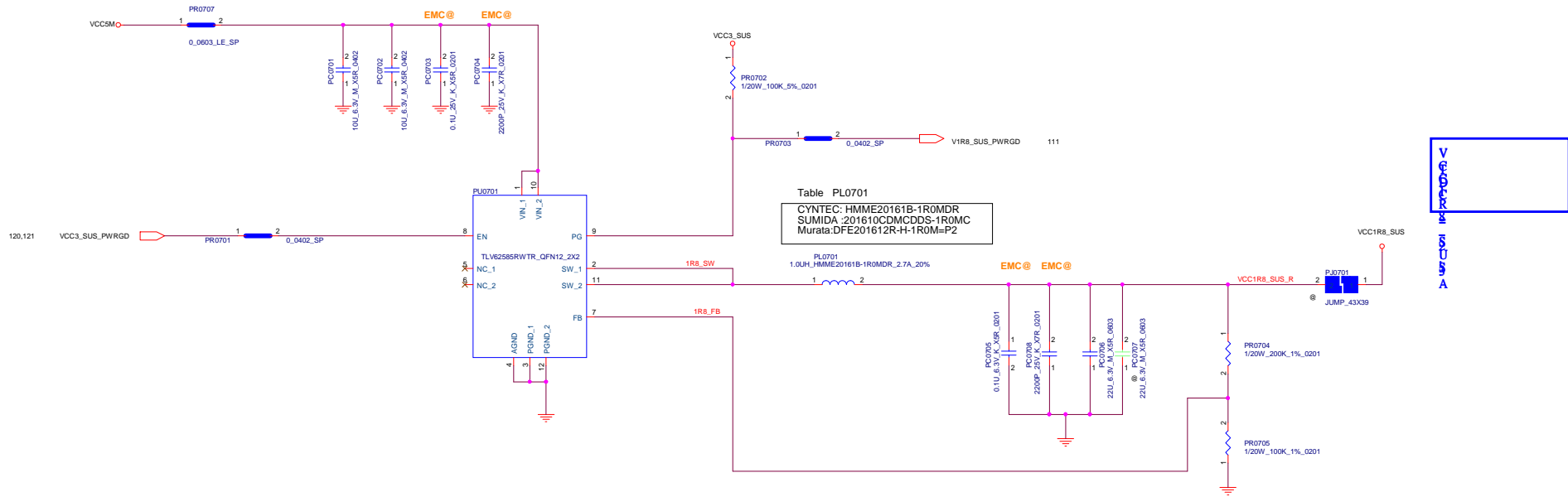


| Mode | VOUT | | RMode |
|------|---------------|-----|----------------|
| M1 | $V_o < 3V$ | DCM | 0 |
| M2 | $V_o < 3V$ | CCM | 90K |
| M3 | $V_o \geq 3V$ | CCM | 150K |
| M4 | $V_o \geq 3V$ | DCM | >230K or Float |

CYNTEC : CMLE053T-1R5MS
SUMIDA :0530CDMCCDS-1R5MC
COILFORCE:CIHP-0530-1R5-MS







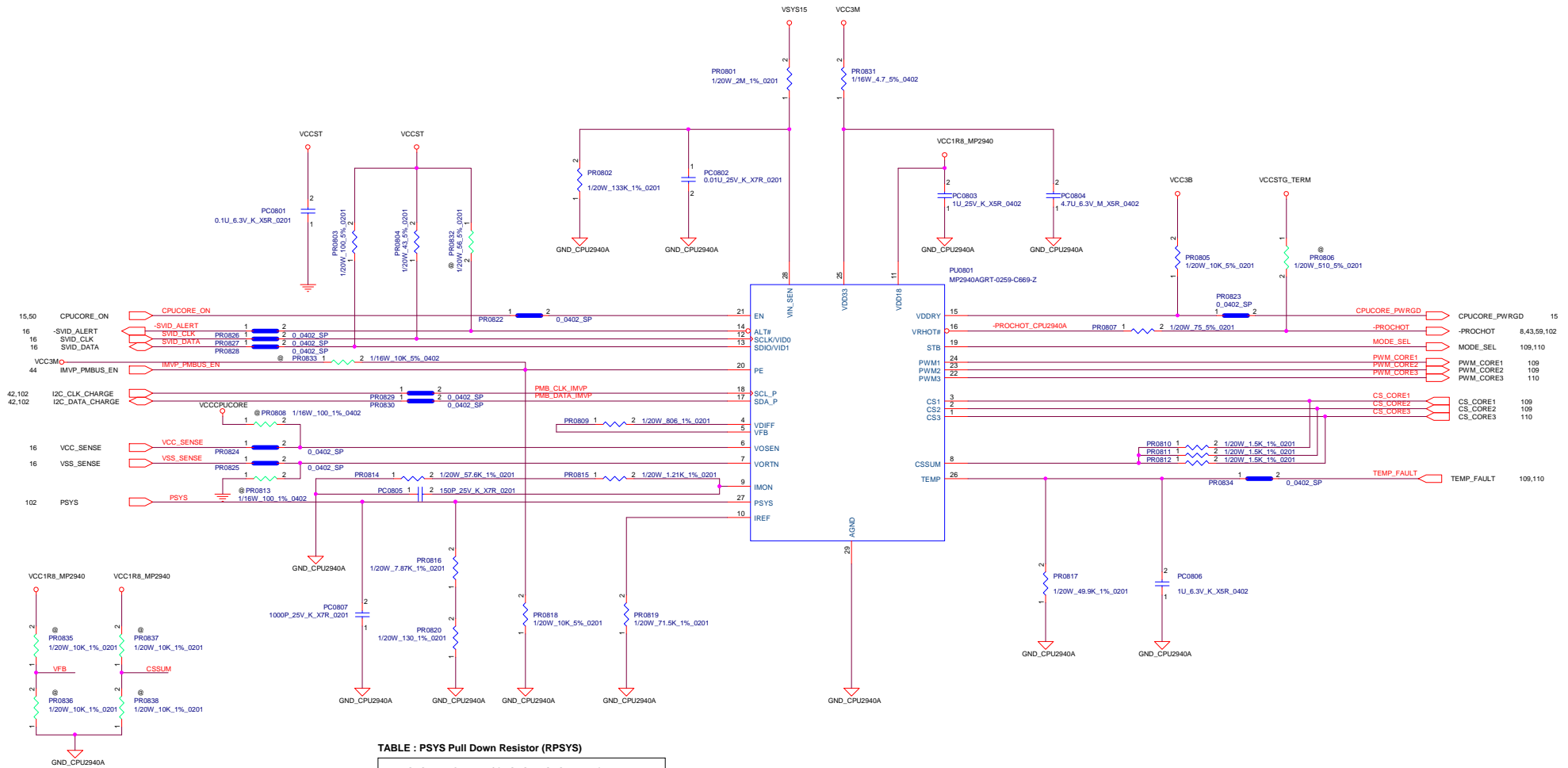
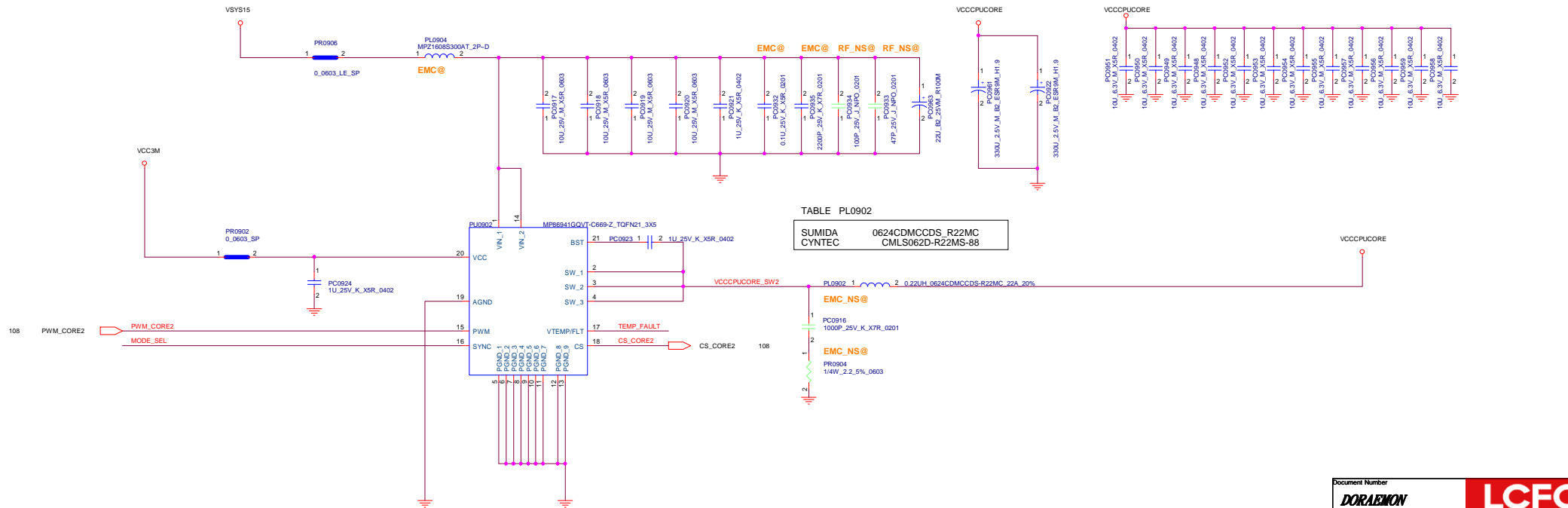
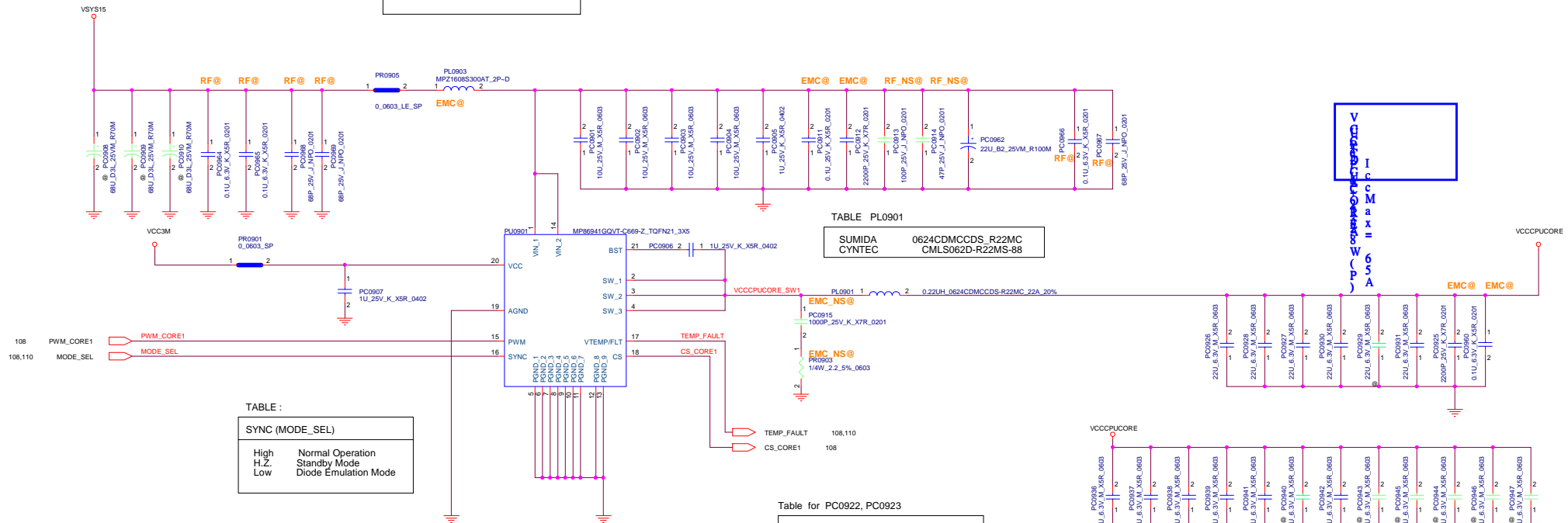


Table PC0908, PC0909, PC0910

Panasonic: 25TQC8MYF
KEMET: T521D686M025ATE070

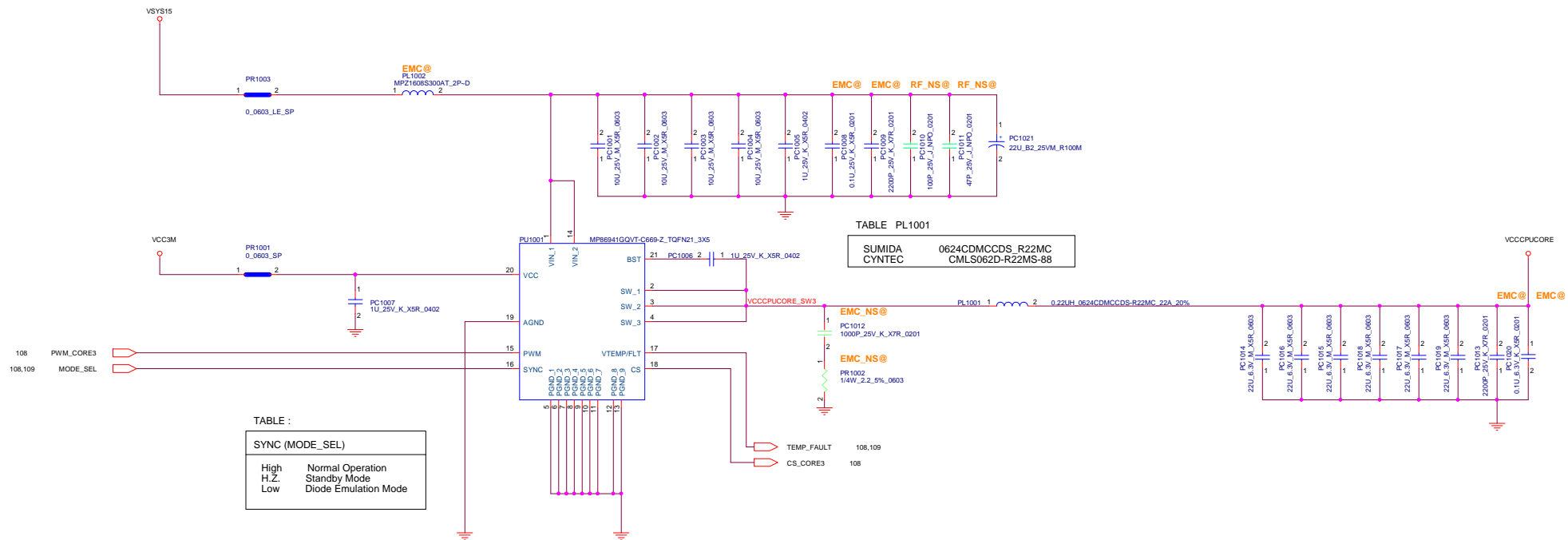


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DORAEON

LCFC

Size: Custom
Title: DC/DC VCCCPUCORE (MP86941 X 2)
Date: Friday, December 18, 2020 Sheet: 109 of 130



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| Size | Title | | | | Rev |
| Custom | DC/DC VCCPCHCORE(MP2941B) | | | | 0.01 |
| Date: | Friday, December 18, 2020 | Sheet | 111 | of | 130 |

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| Custom | <i>DC/DC VCCSM_PD1 (NB693GQ)</i> | 0.01 |
| Date: | Friday, December 18, 2020 | Sheet 113 of 130 |

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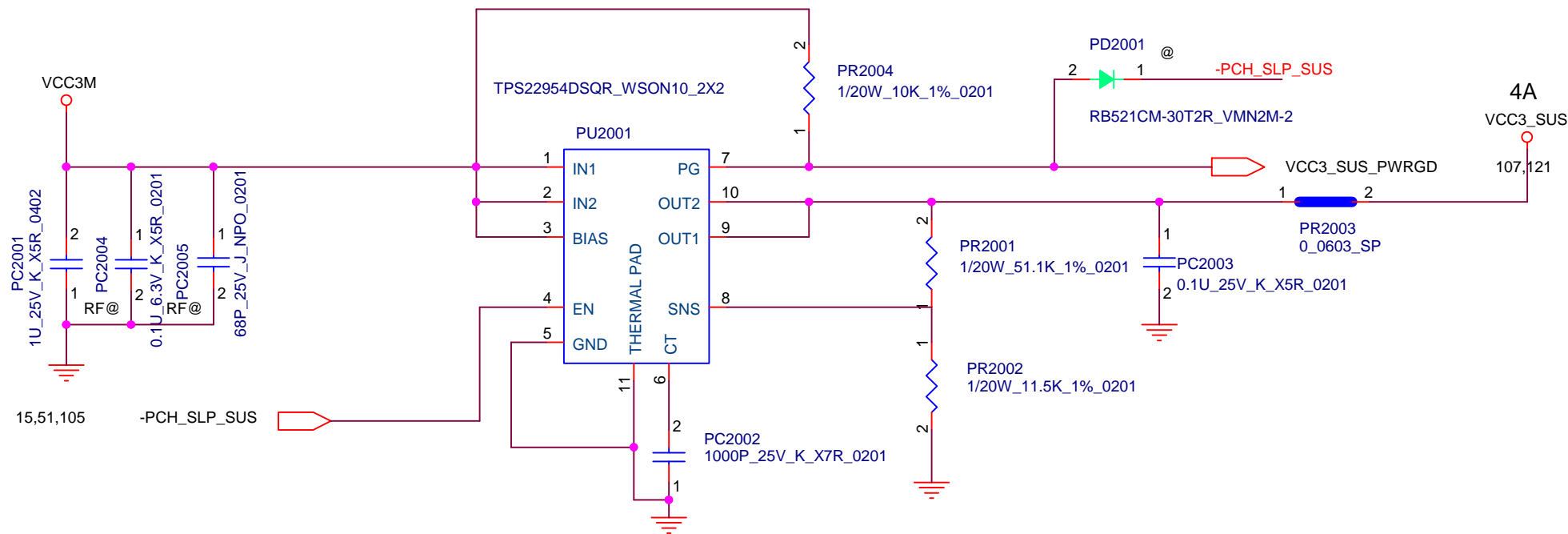
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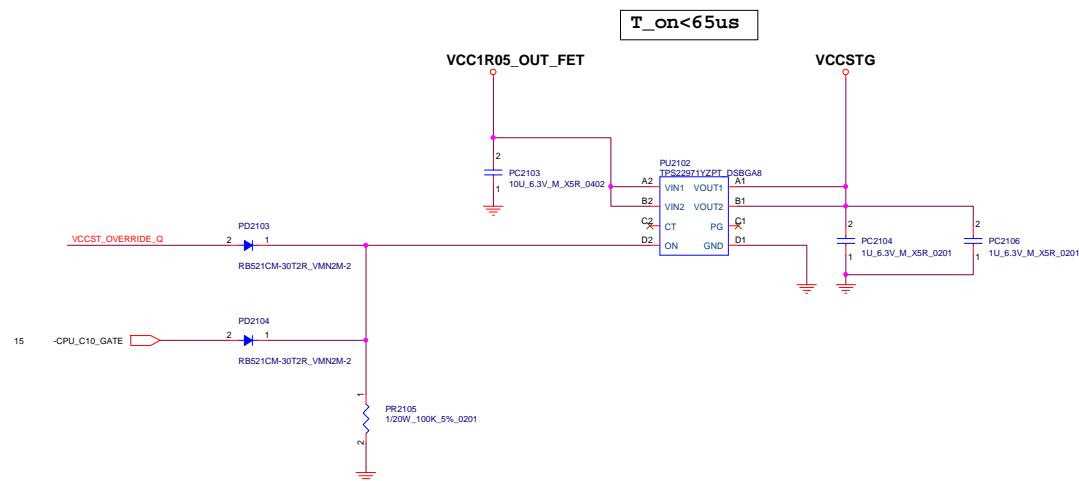
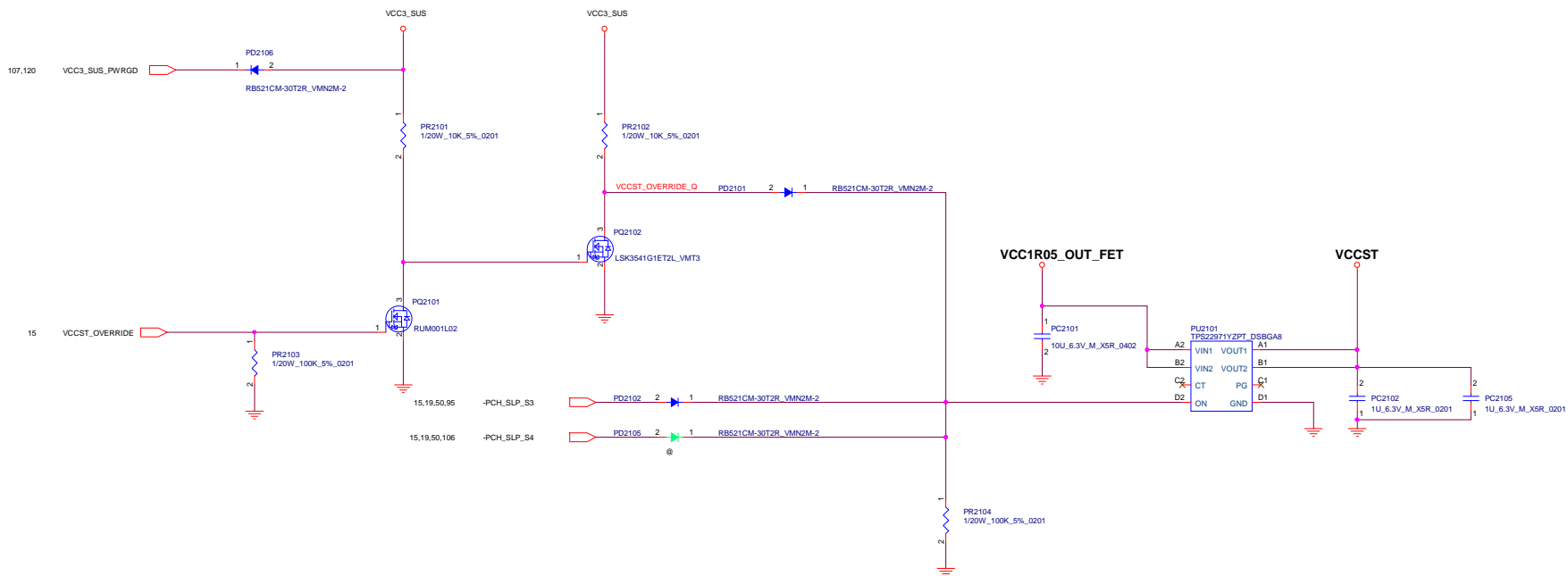
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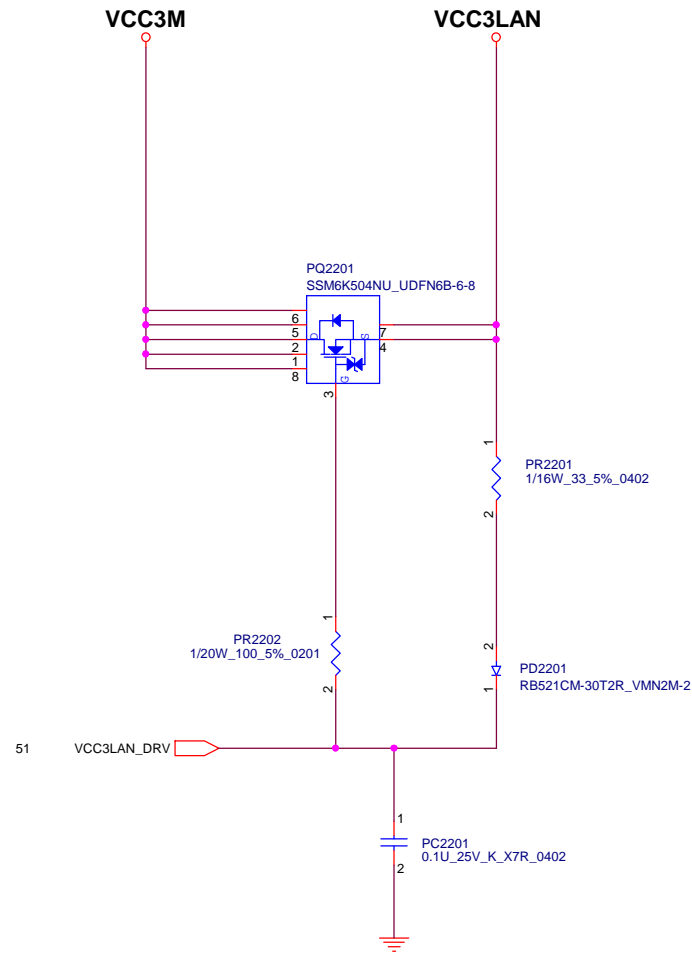
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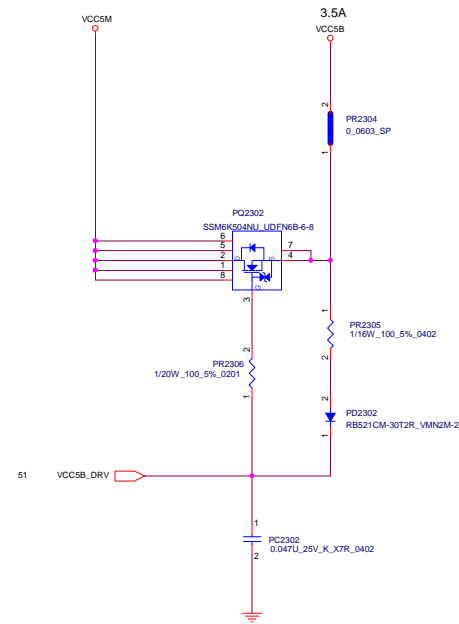
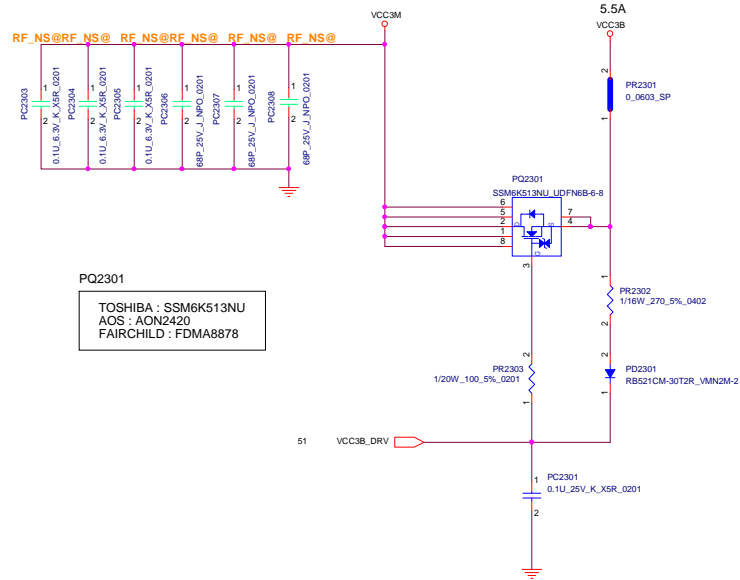




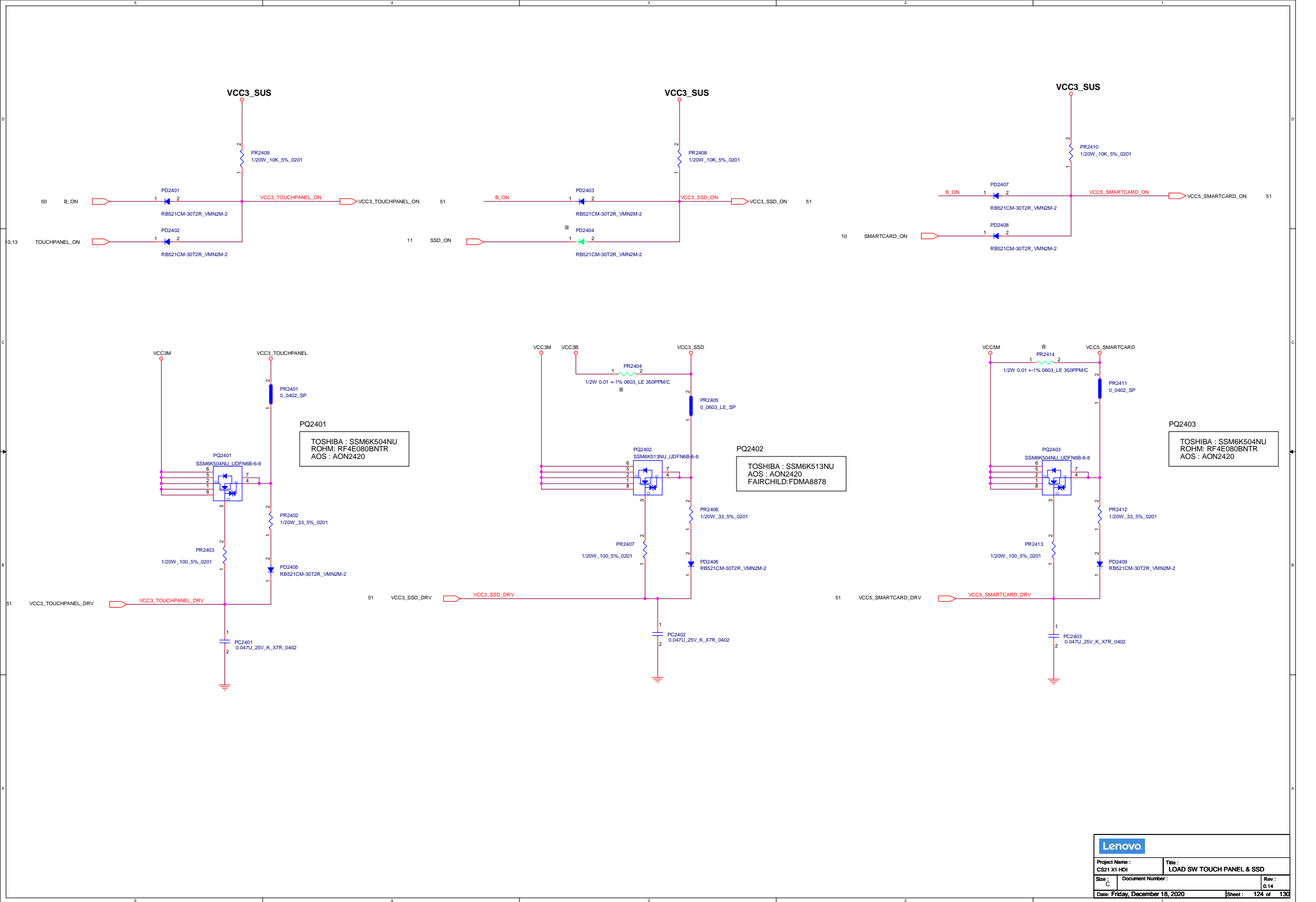
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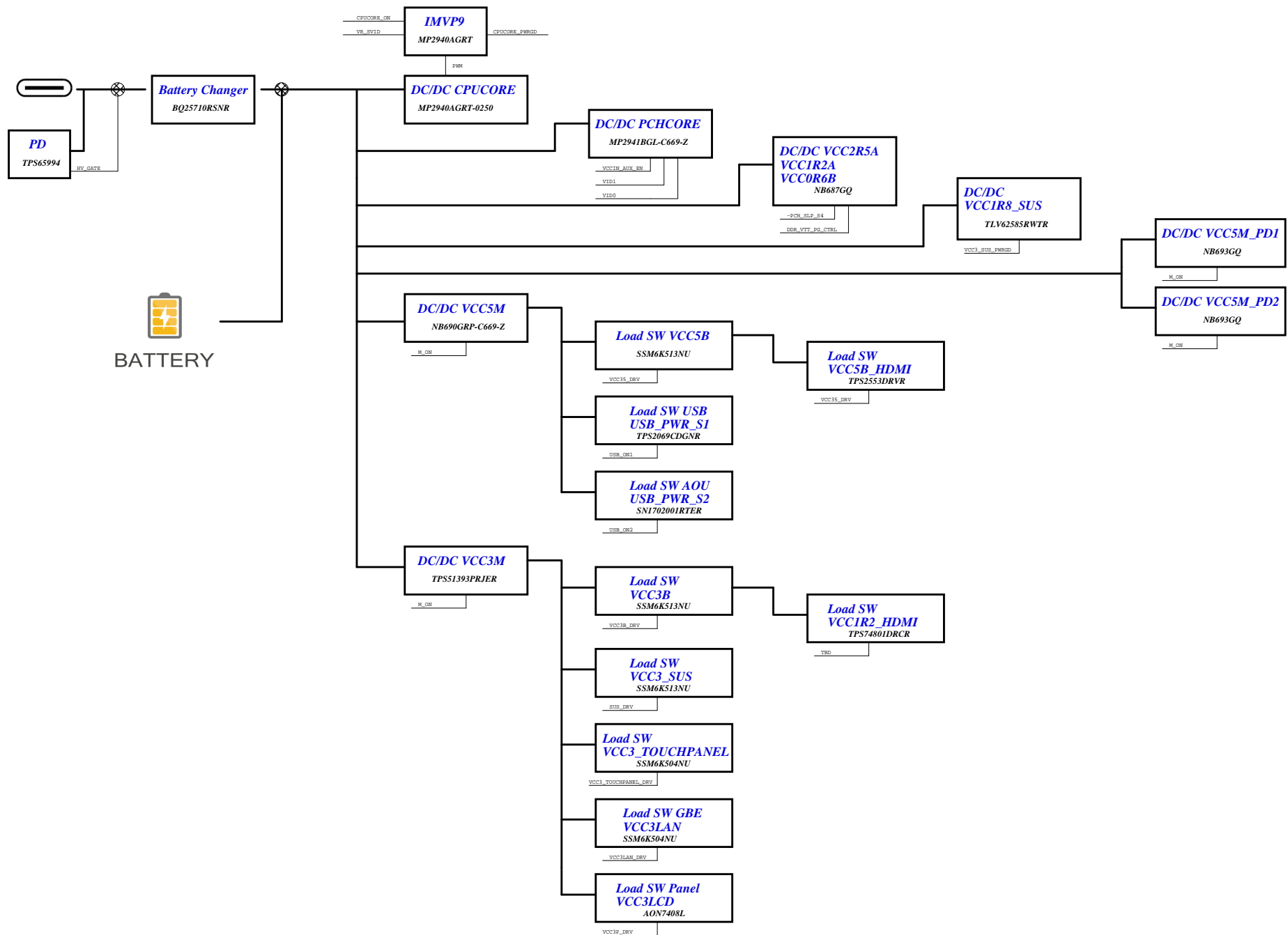
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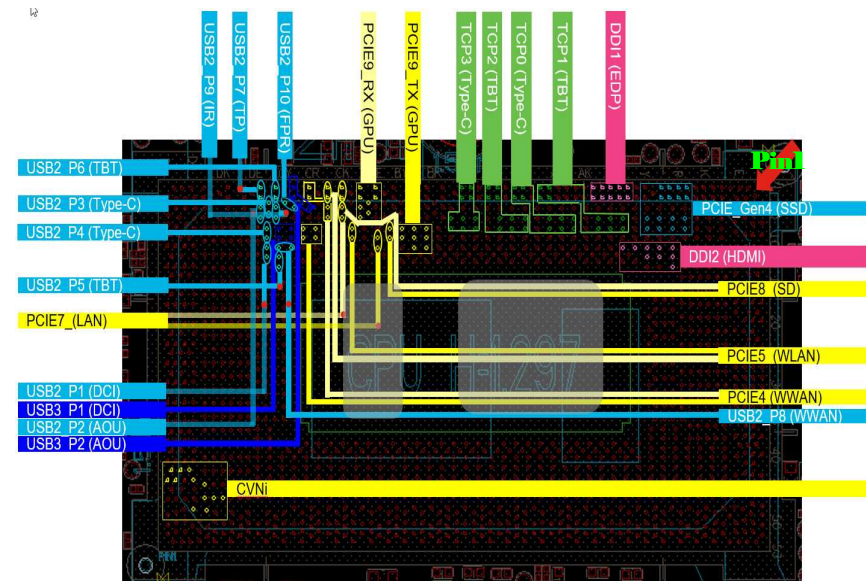
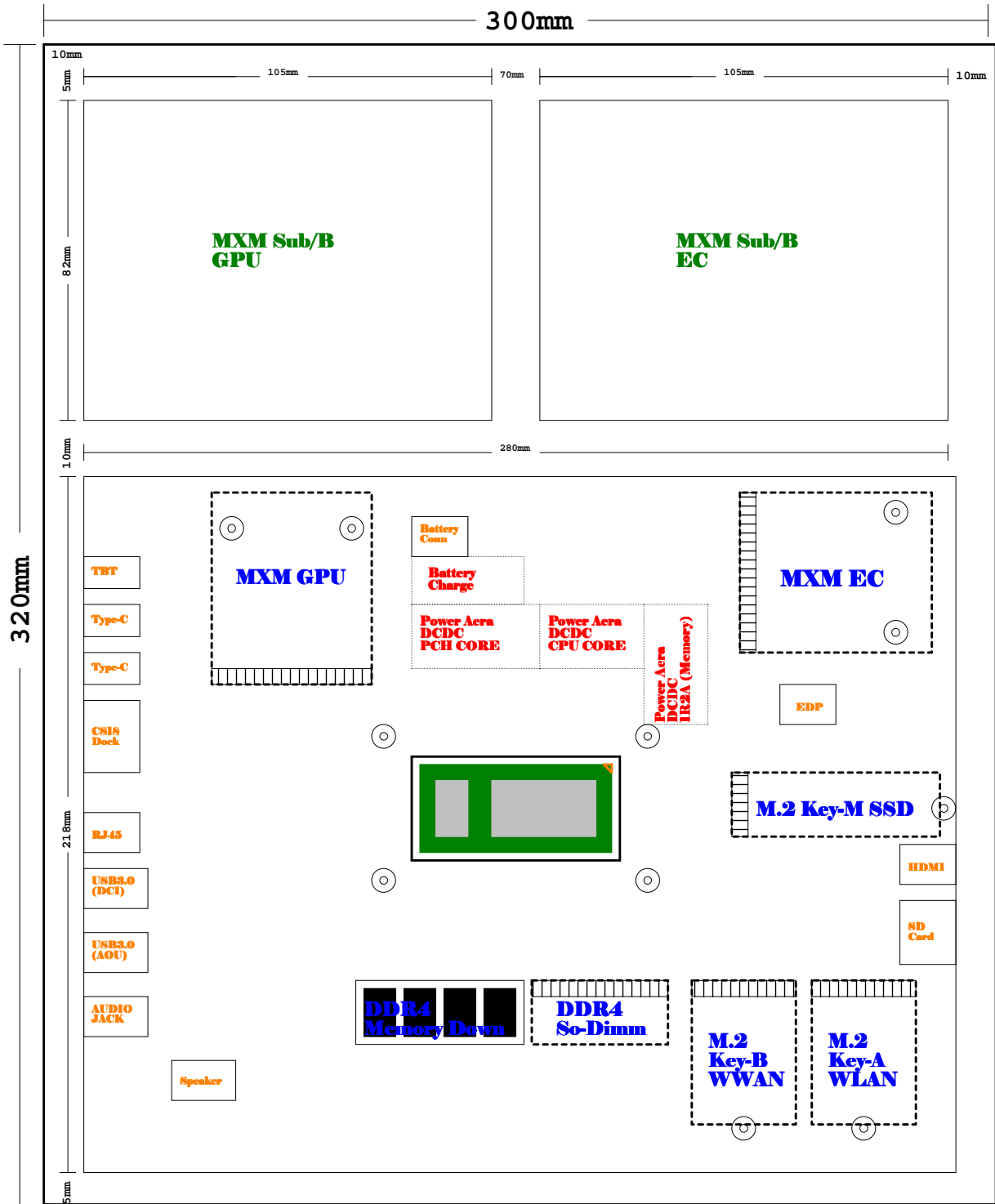
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